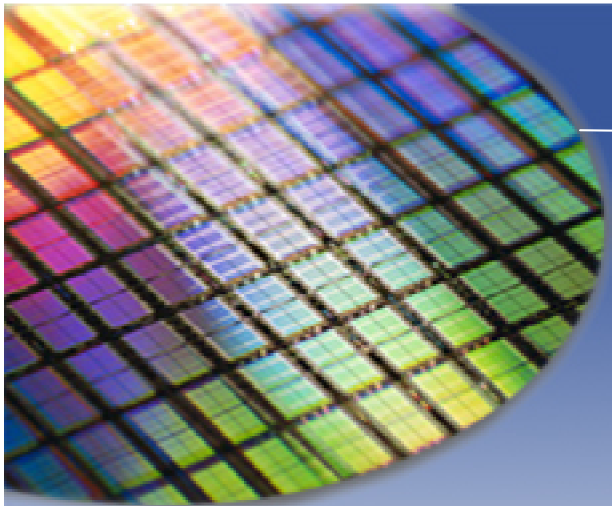


ADI 2006 RF Seminar

Chapter III
RF/IF Components and Specifications for Transmitters

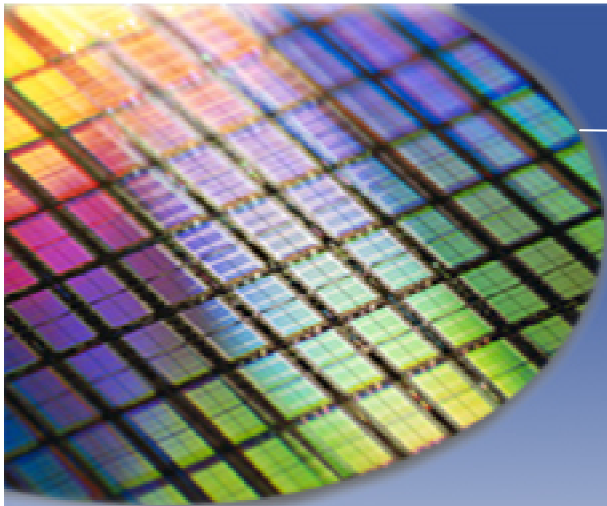
ANALOG DEVICES

RF/IF Components and Specifications for Transmitters

- Transmit DACs
- IQ Modulators
- Amplifiers
- Synthesizers
- RF Power Detectors
- Gain/Phase Detectors
- Vector Modulators

Transmit DACs

- Baseband DACS (usually sold in duals) generate baseband modulated drive signals for IQ Modulators
  - Higher order modulation schemes → higher resolution DACs
  - Higher symbol rates → higher DAC sampling rates
- IF Synthesizing DACS digitally up convert the baseband signal and produce a low Intermediate Frequency either in real form (single DAC) or in complex form (dual DAC)
  - IF Synthesizing DACs → higher performance than Baseband DACs
  - Eliminate the need for one PLL and one mixer
  - Produce better modulation quality (lower EVM)



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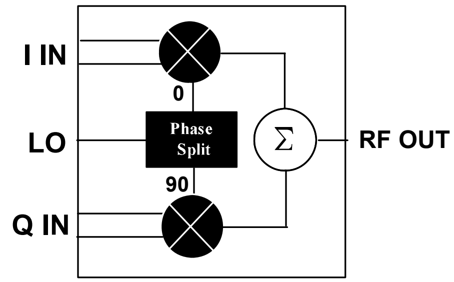
IQ Modulators

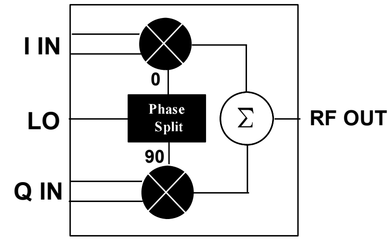
ANALOG DEVICES

RF Components – IQ Modulators



- An un-Modulated Sinewave drives LO input (from PLL). LO is split into "Quadrature" components of equal amplitude but 90 degrees out of phase
- I and Q drive signals are multiplied by LO Quadrature Components and then combined to make IF or RF output
- The phase and amplitude of the output carrier can be adjusted continuously if the amplitude of the I and Q signals is varied (vector modulation)
- For QPSK Modulation, input to I and Q can be a (filtered) Digital Bit Streams of +1 and -1 (not 1 and 0)
- For QAM Modulation, I and Q will be multi-level (driven from DAC)

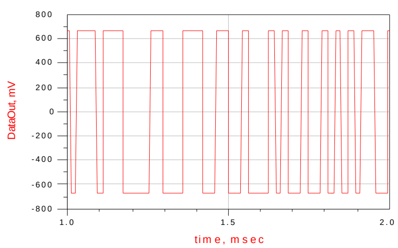
RF Components – IQ Modulators

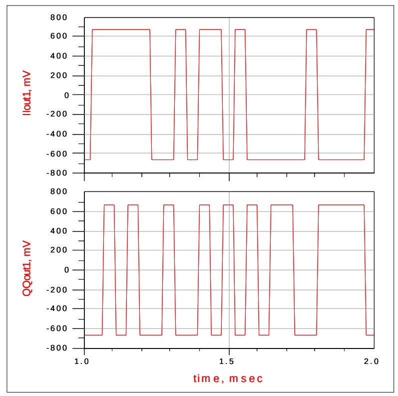


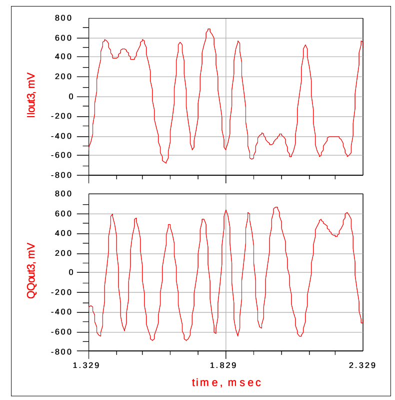
- Critical IQ Mod Specifications
  - Baseband Bandwidth – higher bandwidth allows higher data rate
  - Output Compression Point and Noise Floor – set SNR
  - Quadrature balance of LO Splitter – affects EVM
  - Amplitude balance of LO Splitter – affects EVM
  - LO to RF Out Leakage – adds unwanted component to modulated signal and degrades EVM (is caused by offset voltages on I and Q inputs)
  - Amplitude Balance of I and Q Channels – affects EVM
  - IP2 and IP3 – determine distortion Products that appear in adjacent channels.
  - Amplitude and phase imbalance of any signals affects image suppression in image-reject upconverter

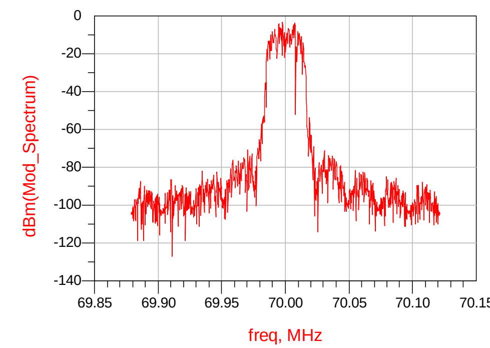
ANALOG DEVICES

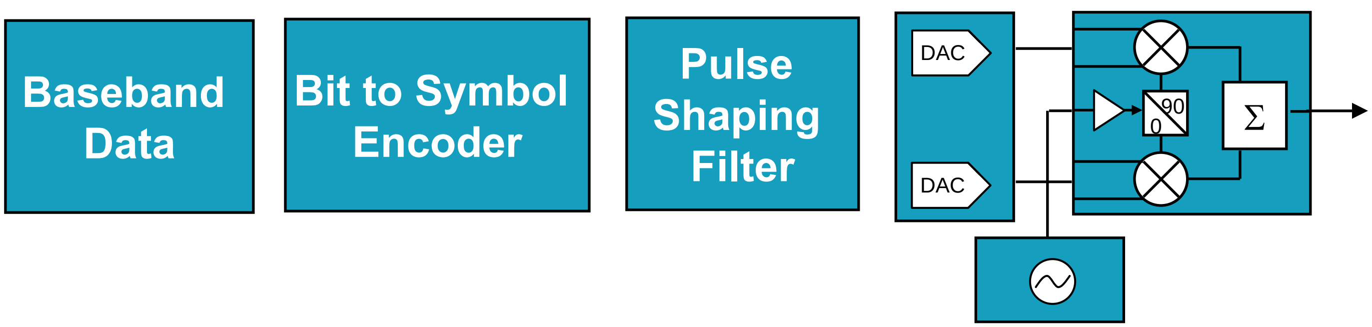
Quadrature Modulation Refresher







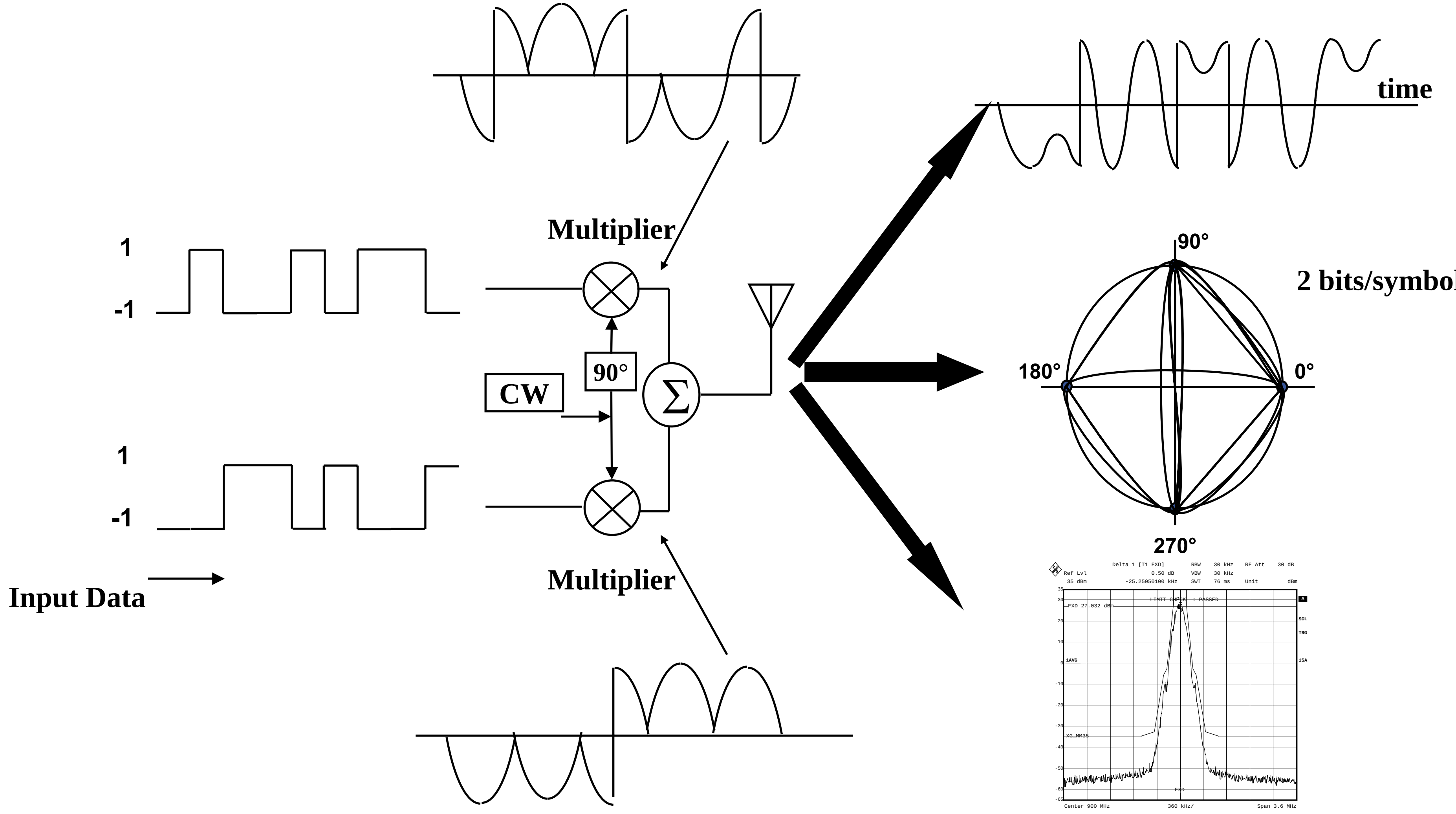




$$RF(t)=A(t)\cos(\omega_c t+\theta(t)) = I(t)\cos\omega_c t + Q(t)\sin\omega_c t$$

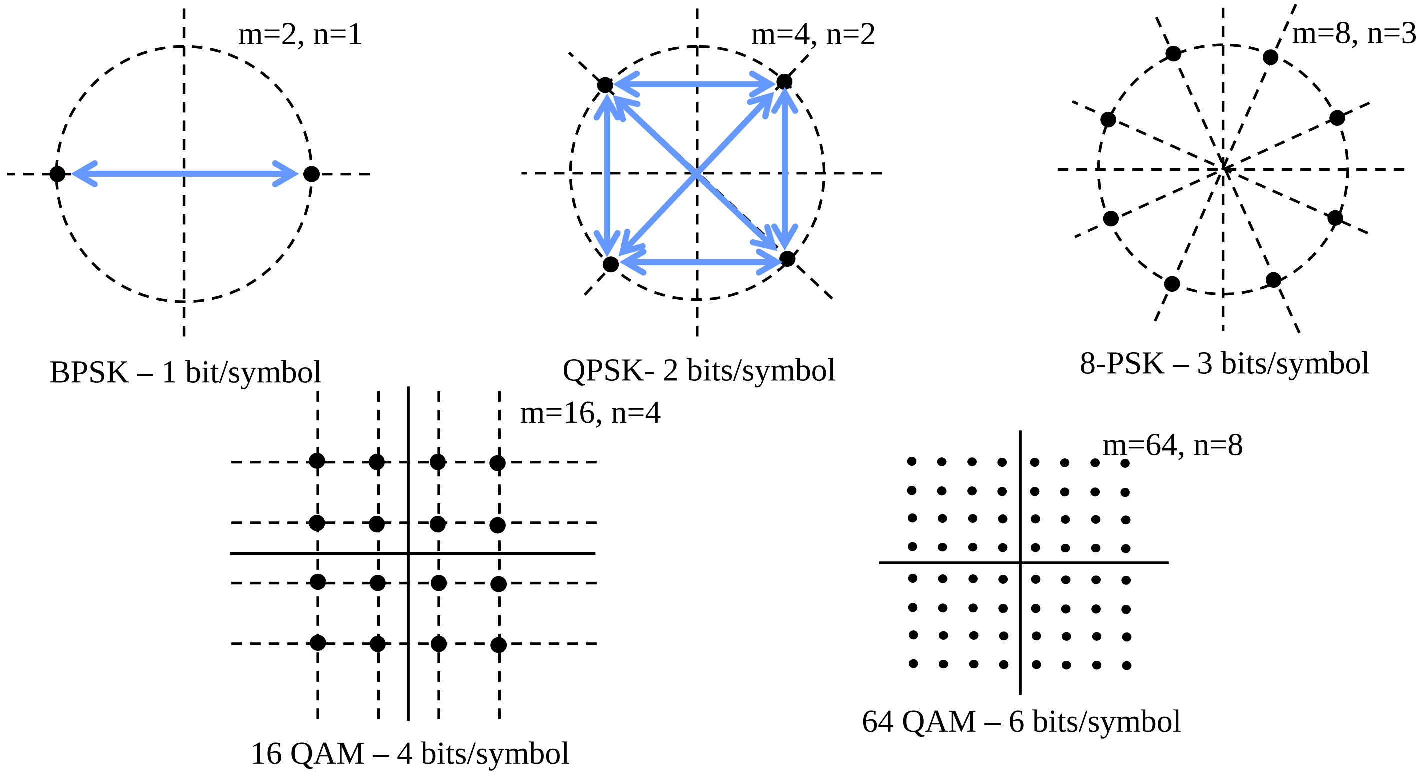
Polar representation   Cartesian representation

Example - Digital Modulation - QPSK



- In Practice bit stream is low pass filtered before modulation to limit the bandwidth of the modulated spectrum

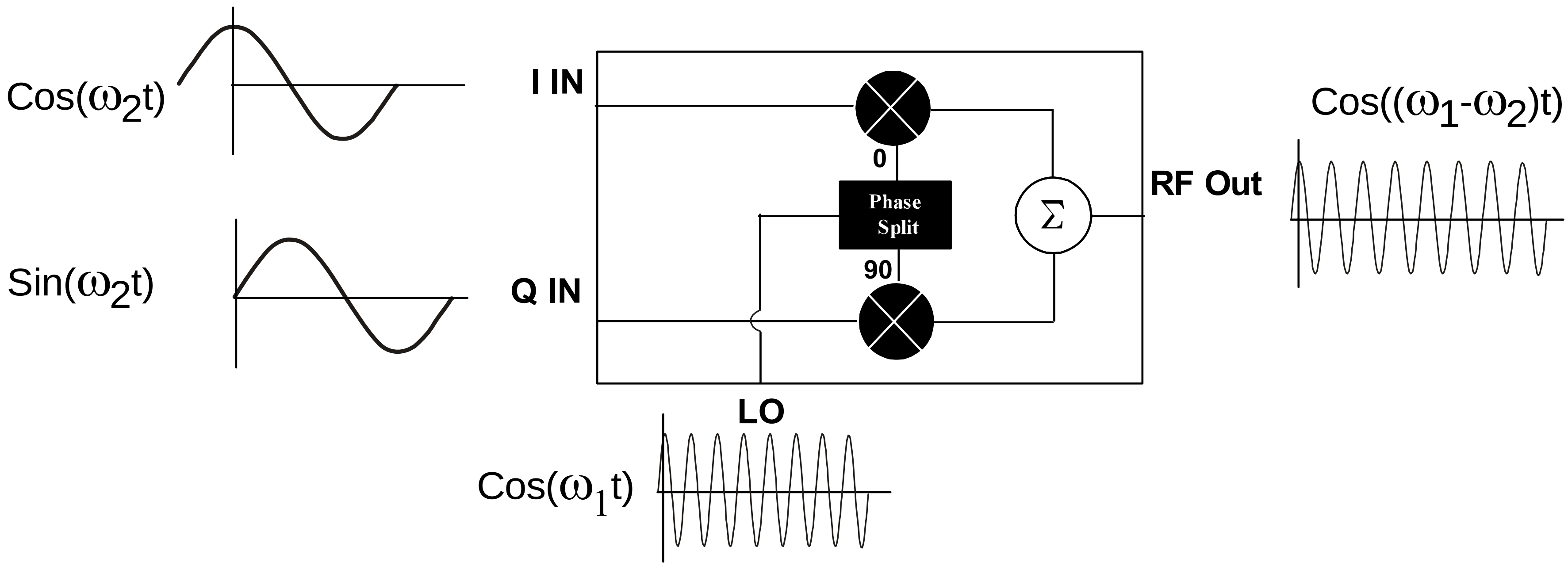
Digital Phase Modulation Schemes



- **Higher Order Modulation Schemes → Higher Data Rate.**
- **But Symbols are closer together → Requires higher Signal-to-Noise Ratio for demodulation**
- **Increasing "Symbol Rate" increases data rate but widens Spectrum**

ANALOG DEVICES

Symbolic Representation of Quadrature Modulator

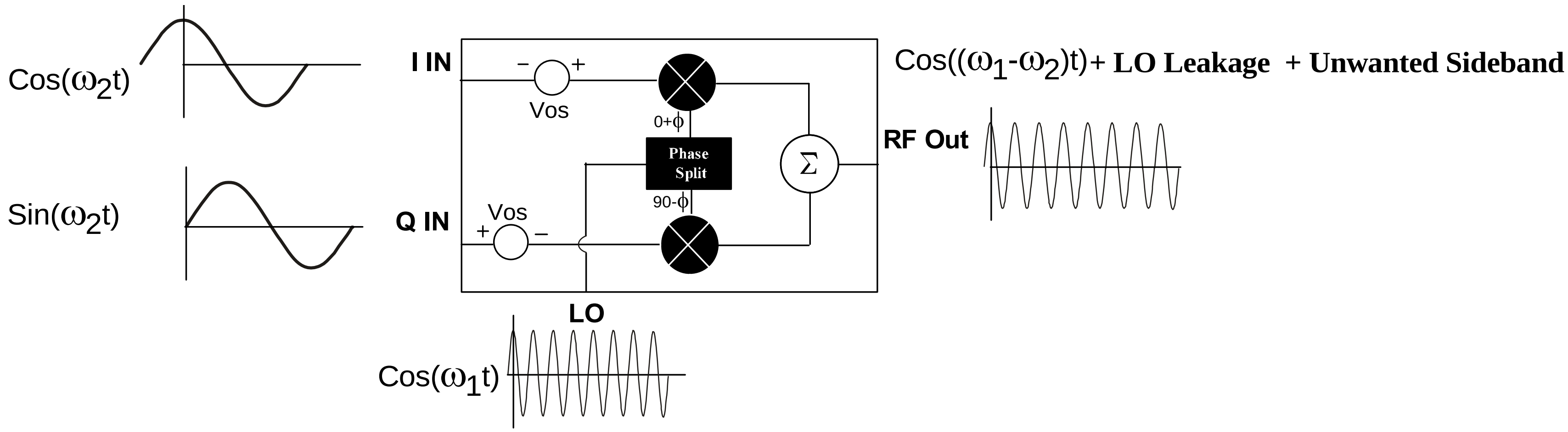


$$Vout = Cos(\omega_1 t)Cos(\omega_2 t) + Sin(\omega_2 t)Sin(\omega_1 t)$$

$$= Cos((\omega_1 - \omega_2)t)$$

- **Local Oscillator signal is split into quadrature components**
- **Mix with quadrature baseband components and you get a single tone at the difference frequency (w_1 -w_2)**

Symbolic Representation of Quadrature Modulator with Errors and Baseband Offset Errors



$$V_{out} = (\cos(\omega_2 t)+V_{os})\cos(\omega_1 t+\phi) + (\sin(\omega_2 t)-V_{os})\sin(\omega_1 t-\phi) =$$

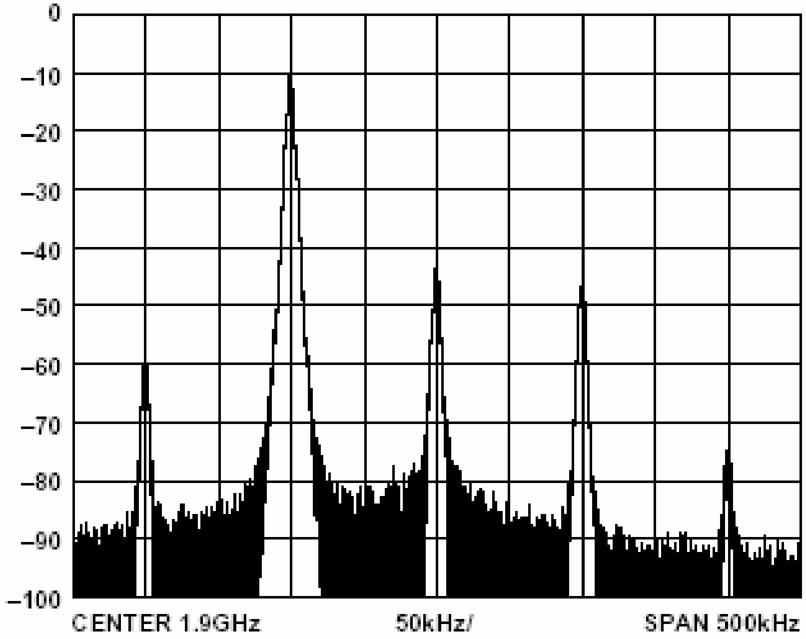
$$= \frac{\cos((\omega_2-\omega_1)t - \phi) + \cos((\omega_2-\omega_1)t + \phi)}{2} +$$ ⟵ Lower Sideband

LO Leakage ⟶ $$V_{os}(\cos(\omega_1 t + \phi) - \sin(\omega_1 t - \phi)) +$$

$$\frac{\cos((\omega_2+\omega_1)t + \phi) - \cos((\omega_2+\omega_1)t - \phi)}{2}$$ ⟵ Unwanted Upper Sideband

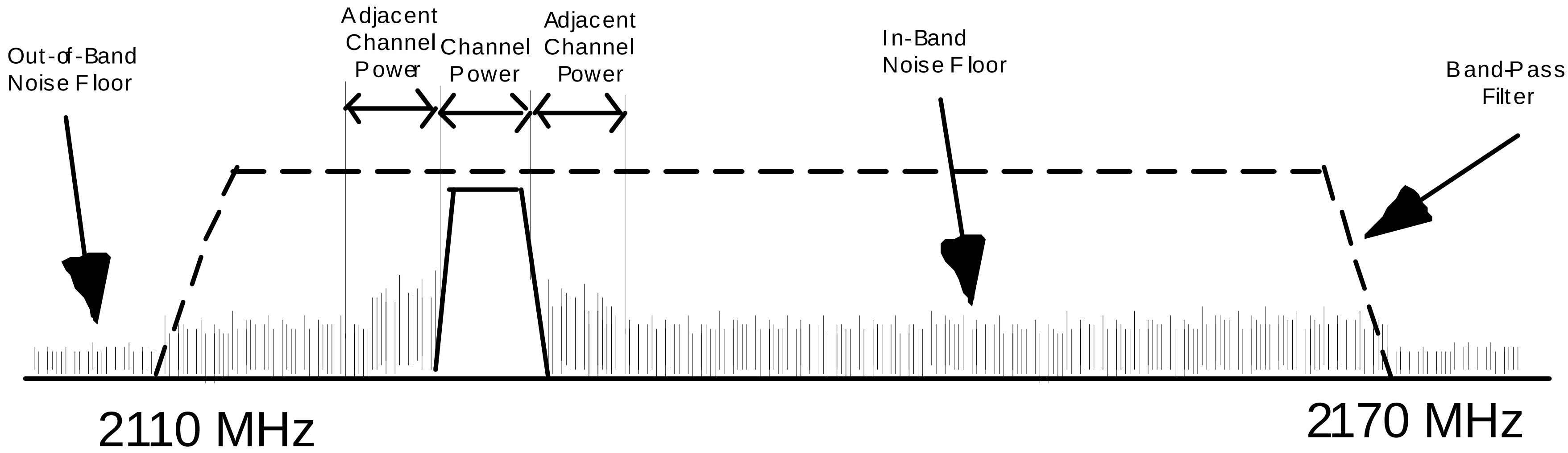
•Baseband amplitude, offset and phase errors along with LO quadrature errors will produce unwanted components at the LO and image frequencies

Upconverted Single Side Band Signal with Lo Leakage and upper Sideband Leakage



- **Baseband Offset Compensation can be used to remove LO Leakage**
- **To remove upper sideband, baseband amplitude and phase compensation is required.**
- **2nd and 3rd order harmonics cannot be easily removed**
- **While Single Sideband Modulation is not used in end-applications, an SSB spectrum gives valuable information about the quality of the WCDMA, CDMA, GMSK, etc spectrum**
- **Excessive LO leakage, Sideband Leakage and harmonics will increase Error Vector Magnitude (EVM)**

Modulator Noise Floor

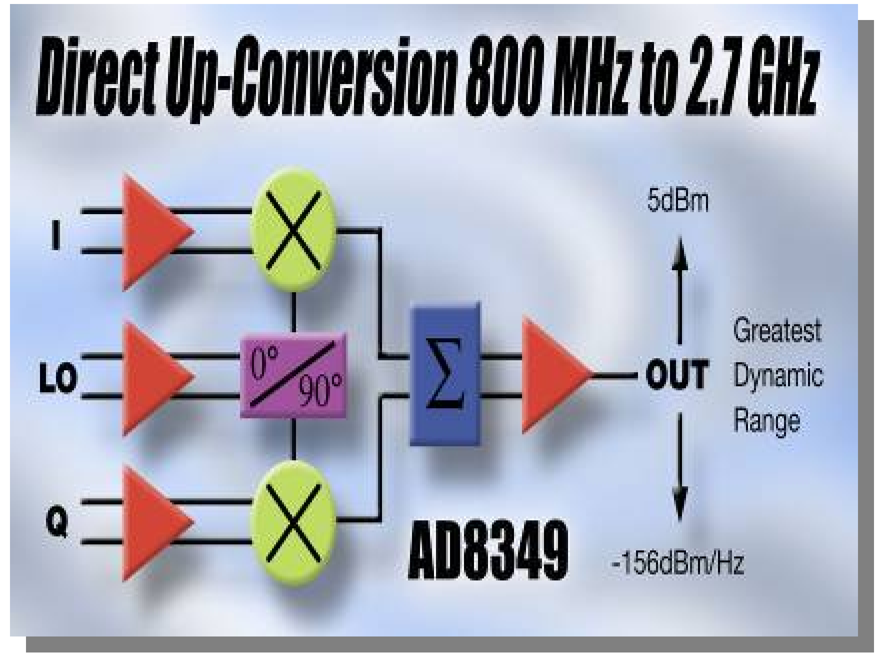


- *Noise of a modulator is typically specified in dBm/Hz (output referred)*
- *Noise (dBm) = Noise floor + 10 log(RBW)*
- *e.g. Noise Floor of –150 dBm/Hz becomes –90 dBm when measured in a 1 MHz Resolution Bandwidth*
- *In-Band Noise cannot be filtered in a Direct Conversion Architecture (Zero IF or Low IF)*
- *Direct Conversion Modulators must be designed for high output power, low distortion and low noise floor*
- *GSM spec calls for a noise floor of –36 dBm (peak-hold, in 100 KHz BW) at the antenna.*
- *Toughest WCDMA spec calls for –30 dBm (in 1MHz BW) noise floor at the antenna*
- *CDMA calls for <-13 dBm dBm (in 1 MHz BW) at either 4 MHz (cell band) or 2.25 MHz (PCS band) carrier offset.*
- *Need to know how much gain (and noise) comes after the modulator to relate modulator noise specs to system requirement*

AD8349 Direct I/Q Modulator

KEY SPECIFICATIONS

- Frequency Range: 700 to 2700 MHz
- Modulation Bandwidth DC-160Mhz
- Accuracy:
  - Phase Error: 0.7°
  - Amplitude Error: 0.1dB
- Sideband Suppression -40dBc
- Noise Floor -156dBm/Hz
- P1dB 7.6 dBm (1900MHz)
- Package 16-TSSOP



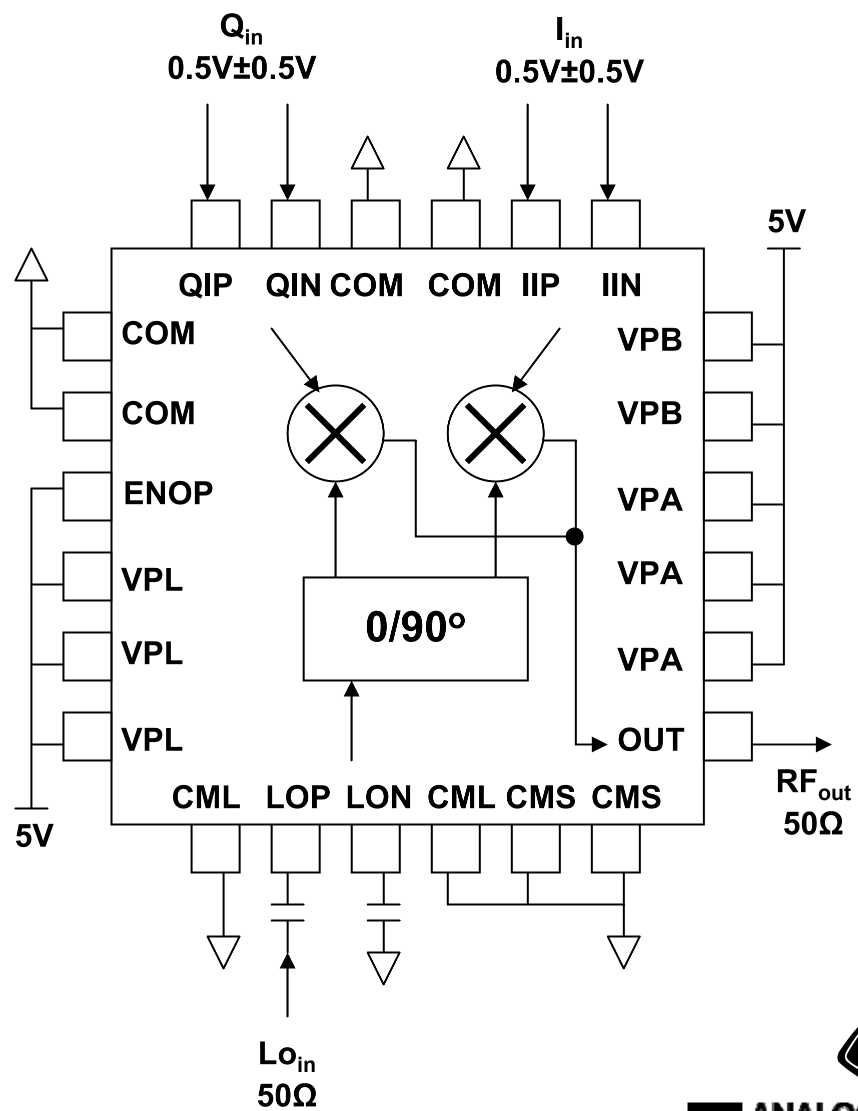
FEATURES

- Matched 50 ohm output
- TxDAC compatible base band inputs
- Output disable function

ANALOG DEVICES

Direct Conversion I/Q Modulators

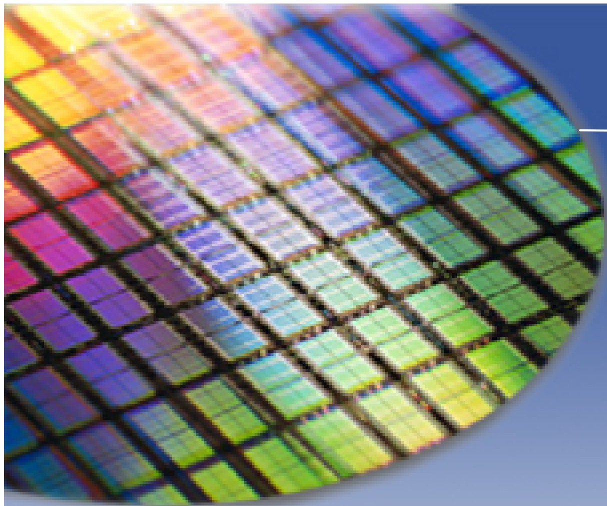
- “FMOD” Family of I/Q Modulators
  - ADL5370 250MHz – 1.3GHz
  - ADL5371 700MHz – 1.3GHz
  - ADL5372 1.6GHz – 2.4GHz
  - ADL5373 2.4GHz – 2.7GHz
  - ADL5374 3.3GHz – 3.8GHz
- OIP3: 24dBm
- Output Noise: -158dBm/Hz
- OP1dB: 11dBm
- Sideband Rejection: >40dBc
- LO leakage: <-40dBm
- LO power: 0dBm
- I/Q Bandwidth: >500MHz
- DC power: 5V, 190mA



I/Q Modulators

Part No.	RF Freq (MHz)	IQ Bandwidth (MHz)	Carrier Suppress (dBm)	Sideband Suppress (dBc)	Noise Floor (dBm/Hz)	P1dB (dBm)	Power Supply (mA)	Package
AD8345	140 to 1000	80	-42	-42	-155	2.5	65	16-lead TSSOP
AD8346	800 to 2500	70	-42	-36	-147	-3	45	16-lead TSSOP
AD8349	700 to 2700	160	-42	-43	-156	6	135	16-lead TSSOP
ADL5390	20 to 2400	230	N/A	N/A	-150	+13	130	24-Lead LFCSP
ADL5385*	50 to 1000	700	-41	-40	-158	+9	250	24-Lead LFCSP
ADL5370-74*	250-3800	500	-40	-40	-158	+11	190	24-Lead LFCSP

* Preliminary Data



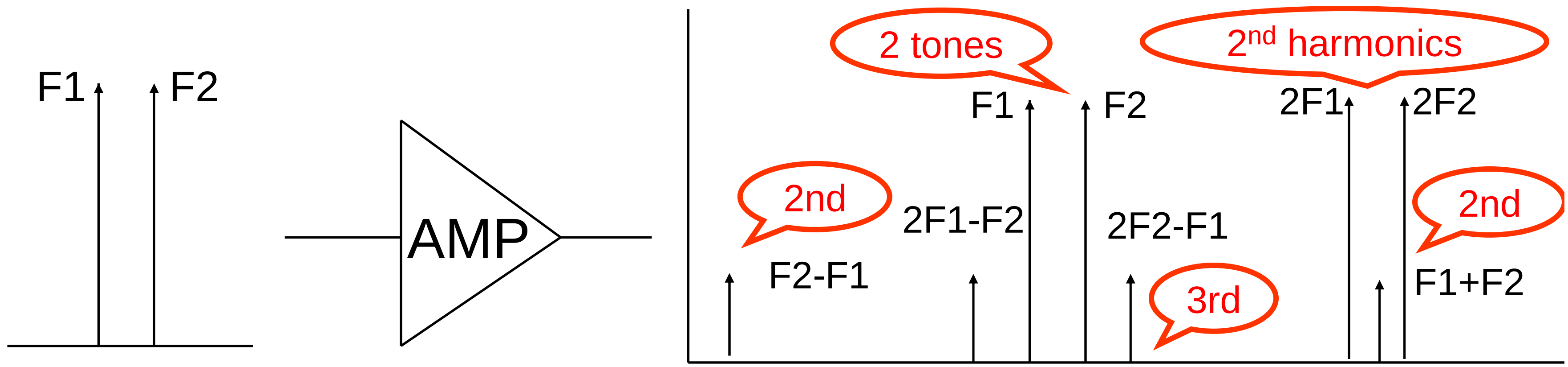
Amplifiers

RF Components – Amplifiers

- **RF Amps**
  - **Input and Output Impedance is 50-1000 Ω**
  - **Fixed or Variable Gain**
  - **Specify Noise as Noise Figure (dB)**
  - **Specify power-handling capability as P1dB**
  - **Specify Intermodulation Distortion as IP2 and IP3**

- **Op Amps**
  - **High Input Impedance**
  - **Very Low Output Impedance**
  - **Gain set using Feedback**
  - **Specify Noise in nV/√Hz**
  - **Specify Voltage Swing (rail-to-rail, etc.)**
  - **Specify Harmonic Distortion in dBc**

Intermodulation Distortion*



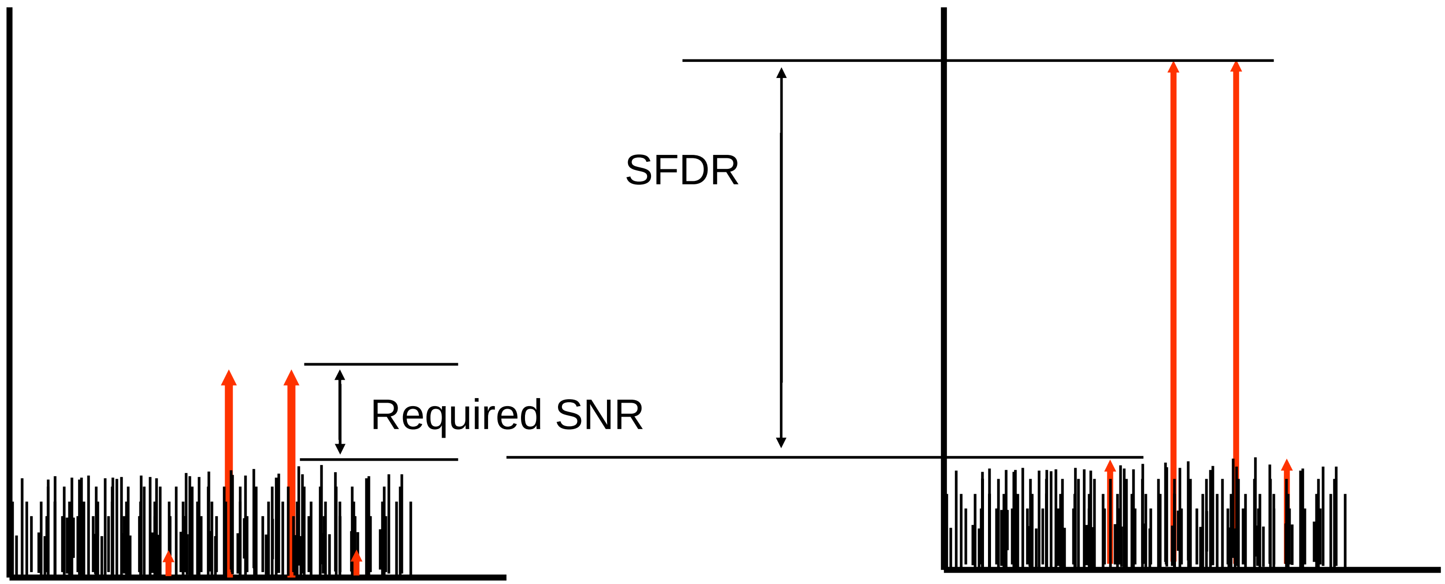
- **IMD products are produced by all active components (mixers, amps, ADCs, DACs)**
- **Third Order IMD Products (close to carrier, nF1+-mF2, n+m=3) are most troublesome**
  - **In Transmitters: IMD causes interference in adjacent channels**
  - **In Receivers: Blocker inter-mod products can fall on the desired signal and de-sensitize the receiver**
- **Second Order IMD Products (F2-F1, n=m=1) cause problems in Direct Conversion Receivers**
  - **Example: Two RF tones 20 kHz apart produce a 20 kHz product at baseband**
- **Two-Tone test is commonly used to predict behavior**

ANALOG DEVICES

Noise

- A background noise power of -174 dBm/Hz is present at every point in a signal chain
- NF = Noise Figure (dB) = 10 log (Noise Factor)
- Noise Power: P = kT (Watts)
  - k = 1.38 x 10^{-23} J/K (Boltzman's constant)
  - T = Kelvin Temperature 298K (25 degC)
- Noise Power (dBm) = 10 log (kT/1mW)
  - = 10 log kT + 30 = -173.9 dBm ≈ -174 dBm
- Noise in a bandwidth B in Hz
  - = -174 dBm/Hz + 10 log B
- Noise Floor, or minimum discernable signal (MDS)
  - = -174 dBm + 10 log B + NF
- Receiver Sensitivity for demodulation at a given carrier to noise (C/N) ratio
  - = -174 dBm + 10 log B + NF + C/N
  - This is the customer's design specification!

Noise & IP3 combine to yield Spurious Free Dynamic Range (SFDR)

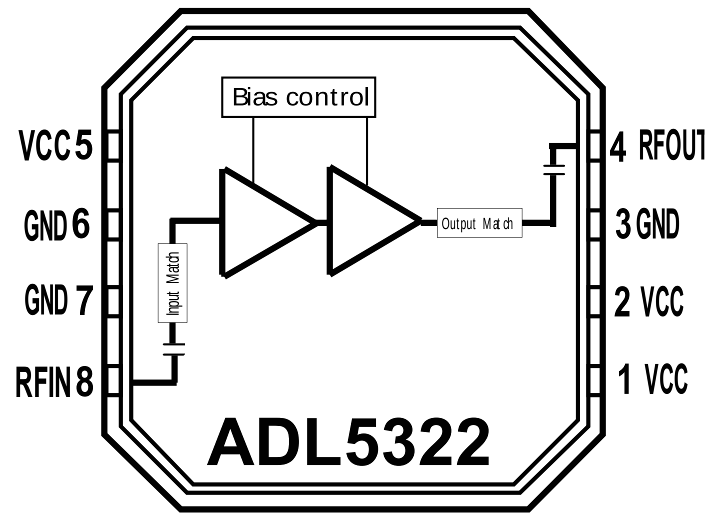


$$SFDR = \tfrac{2}{3}\left[IP3 - Noise\ Floor\right]$$

- Bottom end of SFDR is defined by the required signal-to-noise ratio (to demodulate signal)
- Top end of SFDR is defined by point at which IMD products become equal to noise floor
- SFDR is defined differently for ADCs and DACs

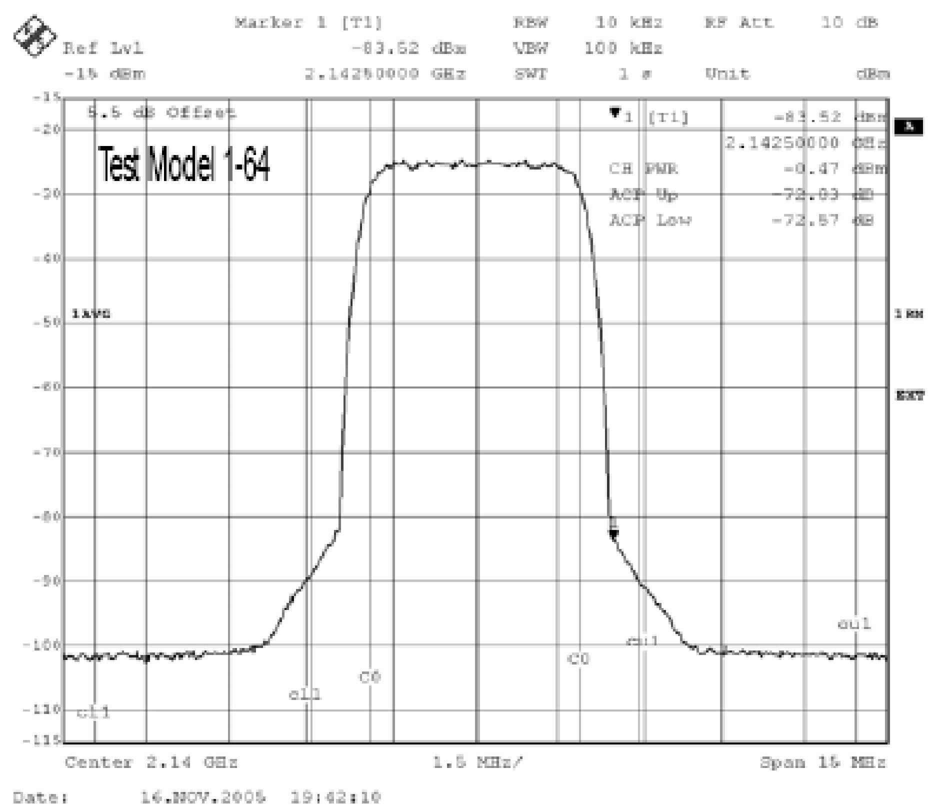
ADL5322/5323 1/2W Driver Amplifiers

- GaAs-based PA drivers with internal matching.
- Operating Frequencies 700-1000 MHz, 1700-2400 MHz
- Gain: 20 dB
- Gain Stable vs. Temp (±0.5dB) and Freq (±0.25dB in-band)
- OIP3: +40/42 dBm
- OP1dB: +27 dBm
- Noise Figure: 4.3/5.1 dB



ADL5323 Single Carrier ACPR

- ❑ **Low and Noise and Low Distortion results in very low Adjacent Channel Power Leakage**
- ❑ **Reducing Output Power will improve Distortion but will degrade SNR**



ANALOG DEVICES

ADL5330 1MHz to 3GHz Variable Gain Amplifier

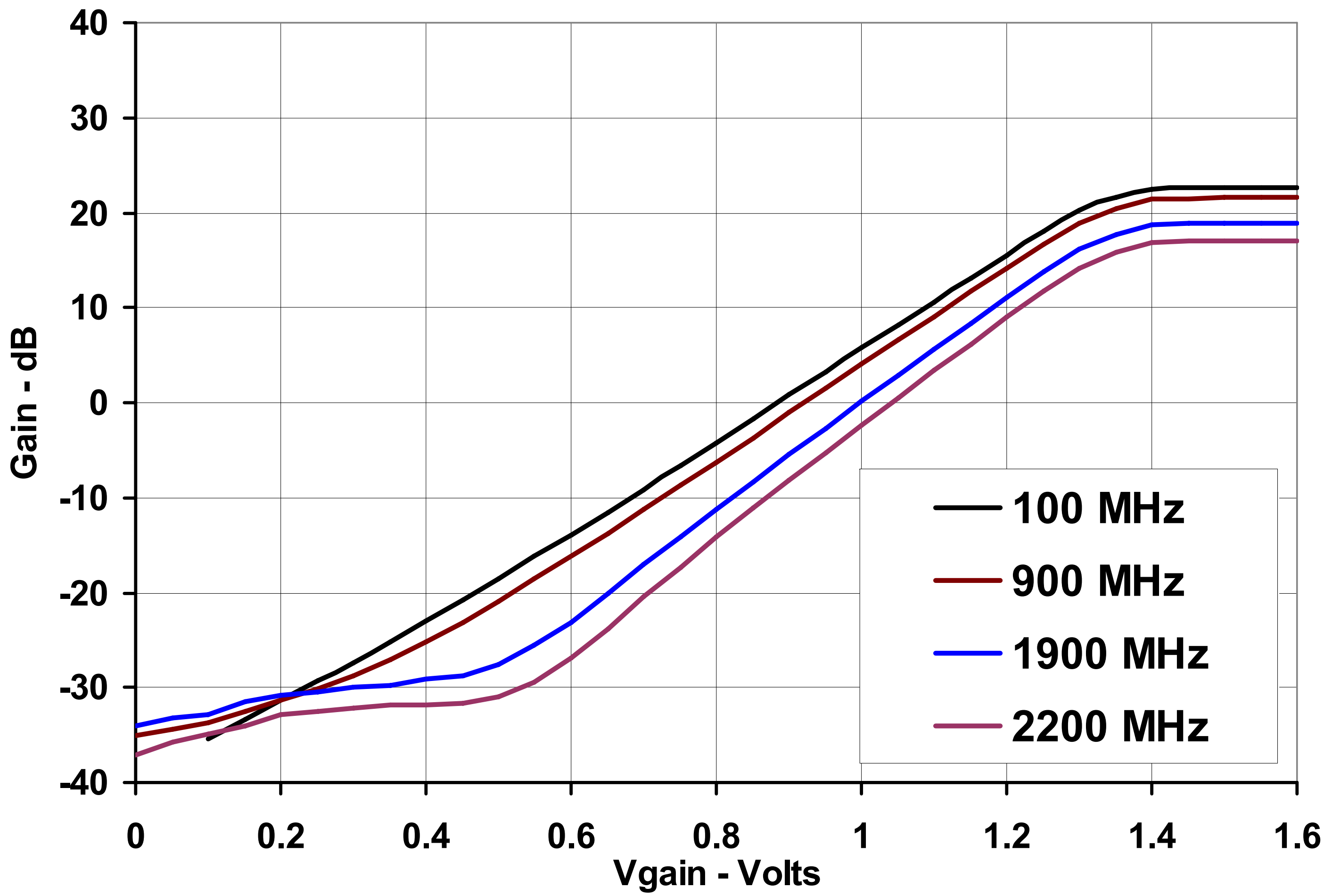
KEY SPECIFICATIONS

- Frequency Range 1MHz to 3GHz
- OIP3 31 dBm @ 900 MHz
- Output Noise Floor -150 dBm/Hz
- 50Ω Differential or Single-Ended Input
- Gain Control Range: -34 dB to +22 dB @ 900 MHz
- Package 4x4mm 24-LFCSP

FEATURES

- Voltage-Controlled Amplifier/Attenuator
- Optimized for Controlling Output Power
- Fully-Balanced Differential Signal Path
- Linear-in-dB Gain Control Function, 20 mV/dB

ADL5330: 1MHz to 3GHz VGA
Gain vs. Gain Control Voltage



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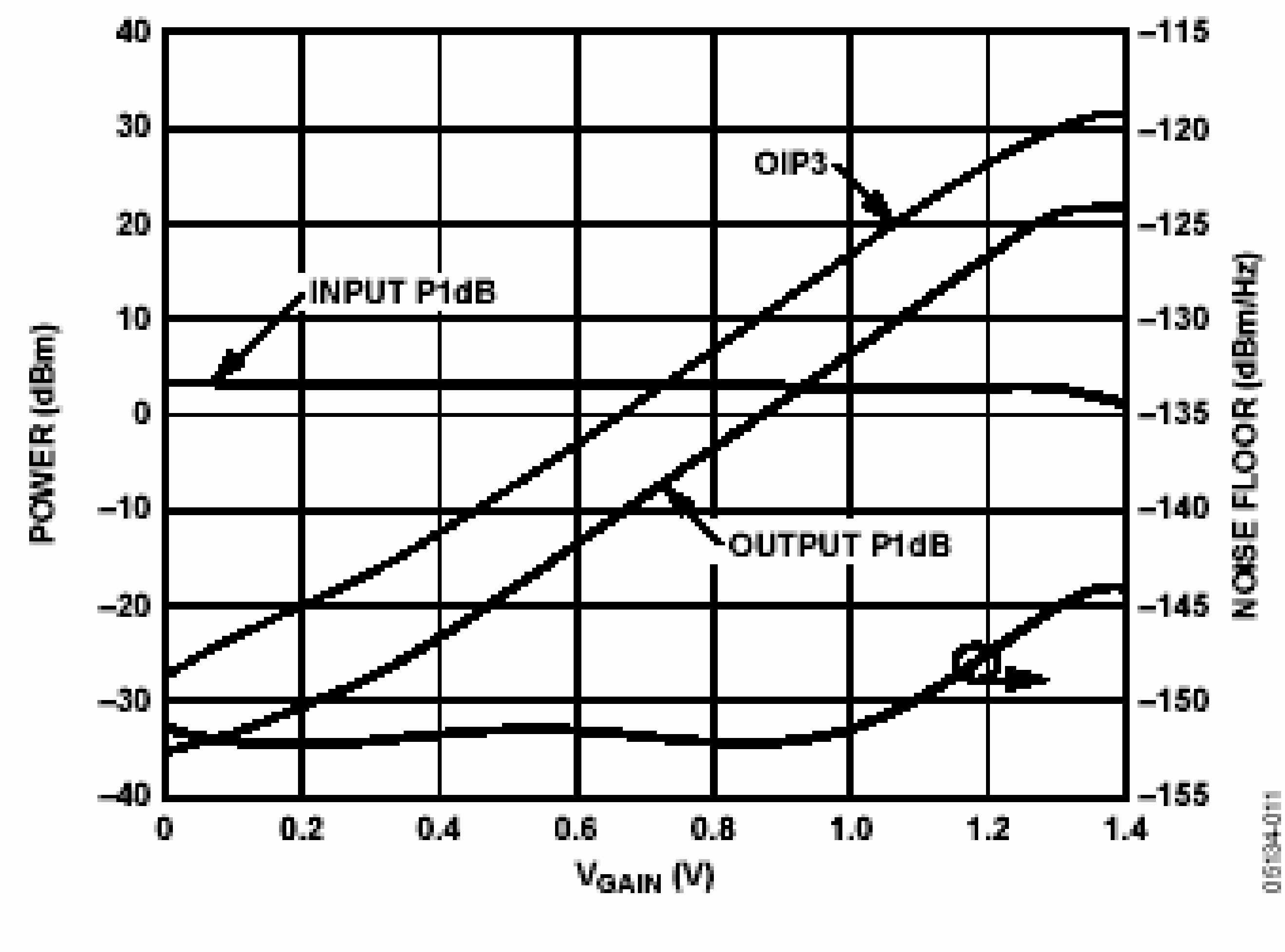
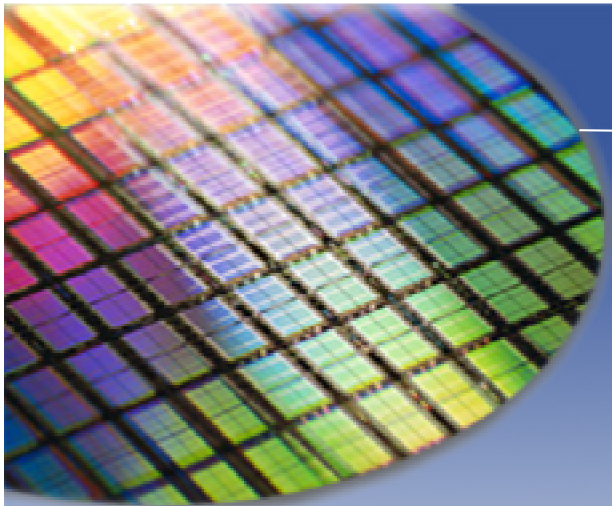
ADL5330: 1MHz to 3GHz VGA

OIP3, P1dB and Noise Floor vs. Gain @ 900 MHz



RF/IF Transmit Amplifiers

Part#	*Freq Range (MHz)*	Gain (dB)	*Output IP3 (dBm)*	Output P1dB (dBm)	Noise Figure (dB)	Comments
AD8353	*1 to 2700*	20	*23.6*	9.1 (900 MHz)	5.3	Rx or Tx
AD8354	*1 to 2700*	20	*19*	4.8 (900 MHz)	4.2	Rx or Tx
ADL5322	*700-1000*	20	*42*	27	5.1	Matched Driver Amp
ADL5323	*1700-2400*	20	*40*	27	4.3	Matched Driver Amp
ADL5330	*1-3000*	-34 to +22	*31*	22	8	Tx VGA



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Oscillators and PLLs

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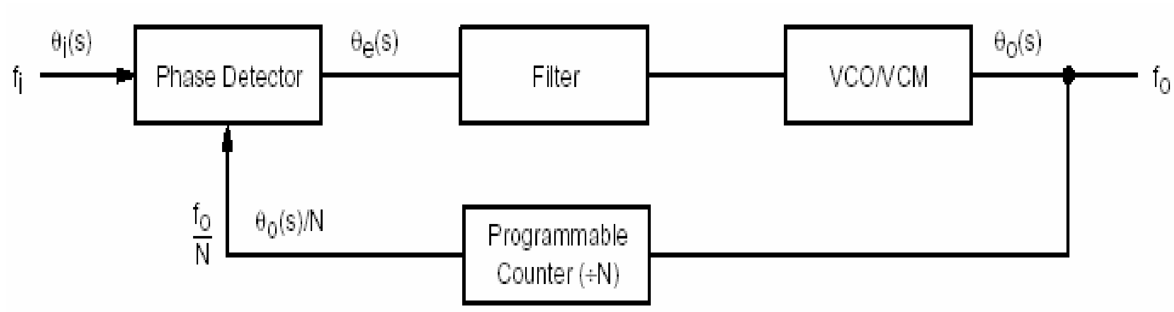
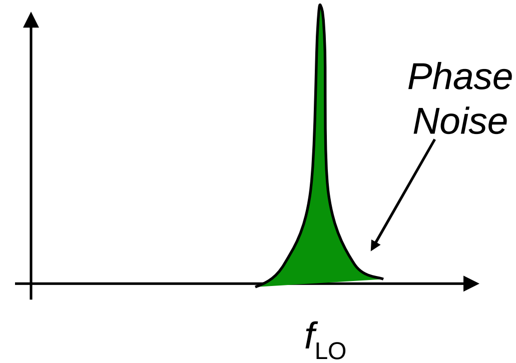
RF Components – Oscillators and PLLs

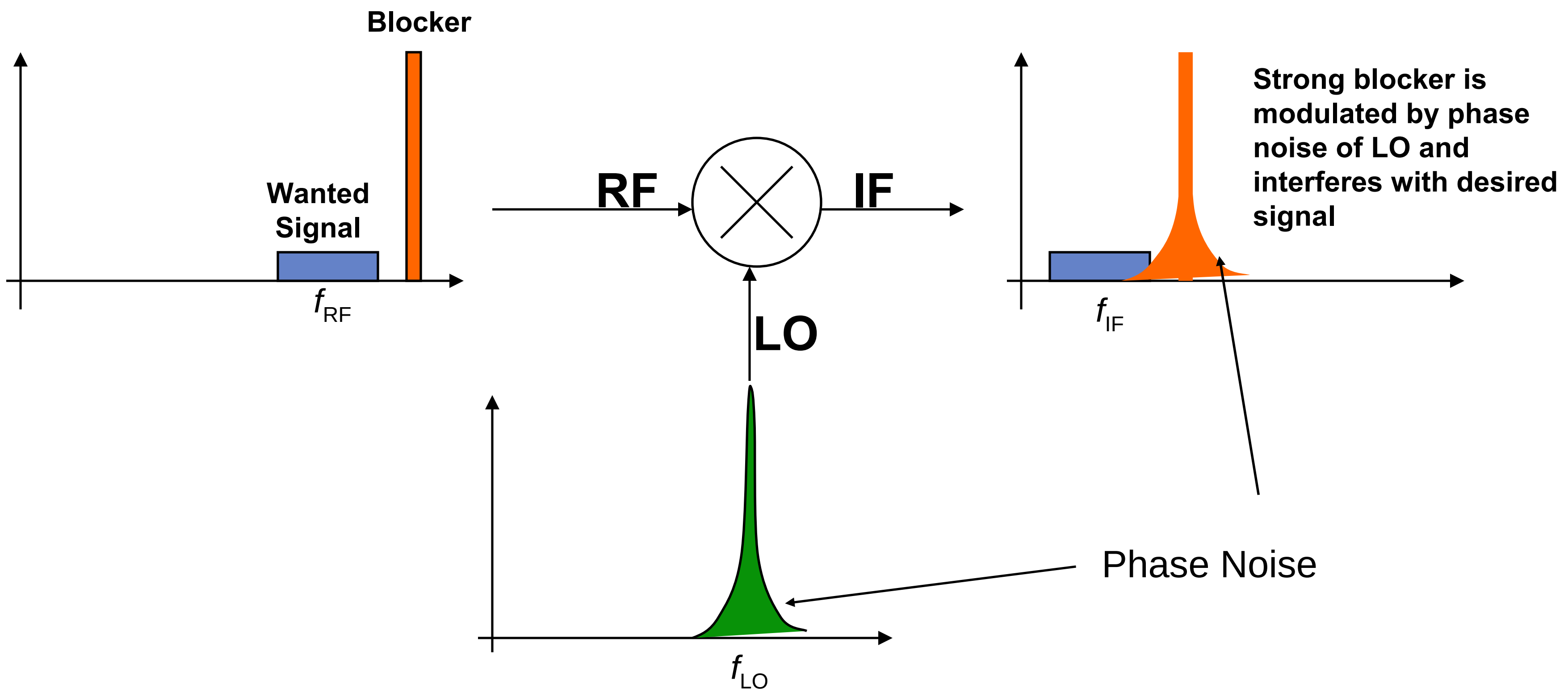


$f_{REF}/R = f_0/N$



- **Phase Locked Loops convert a reference frequency f_{REF} to a higher frequency f_0, which is highly stable**
- **Integer-N PLLs produce an output frequency that is an integer multiple of the reference frequency**
- **Fractional-N PLLs can produce an output which is not an integer multiple of the reference frequency (N can now have a fractional component)**
- **Phase noise and lock time are a PLL's most critical specifications**
- **Output frequency is generated by a Voltage Controlled Oscillator (VCO) which may be integrated with the PLL (ADF4360) at the cost of degraded phase noise**

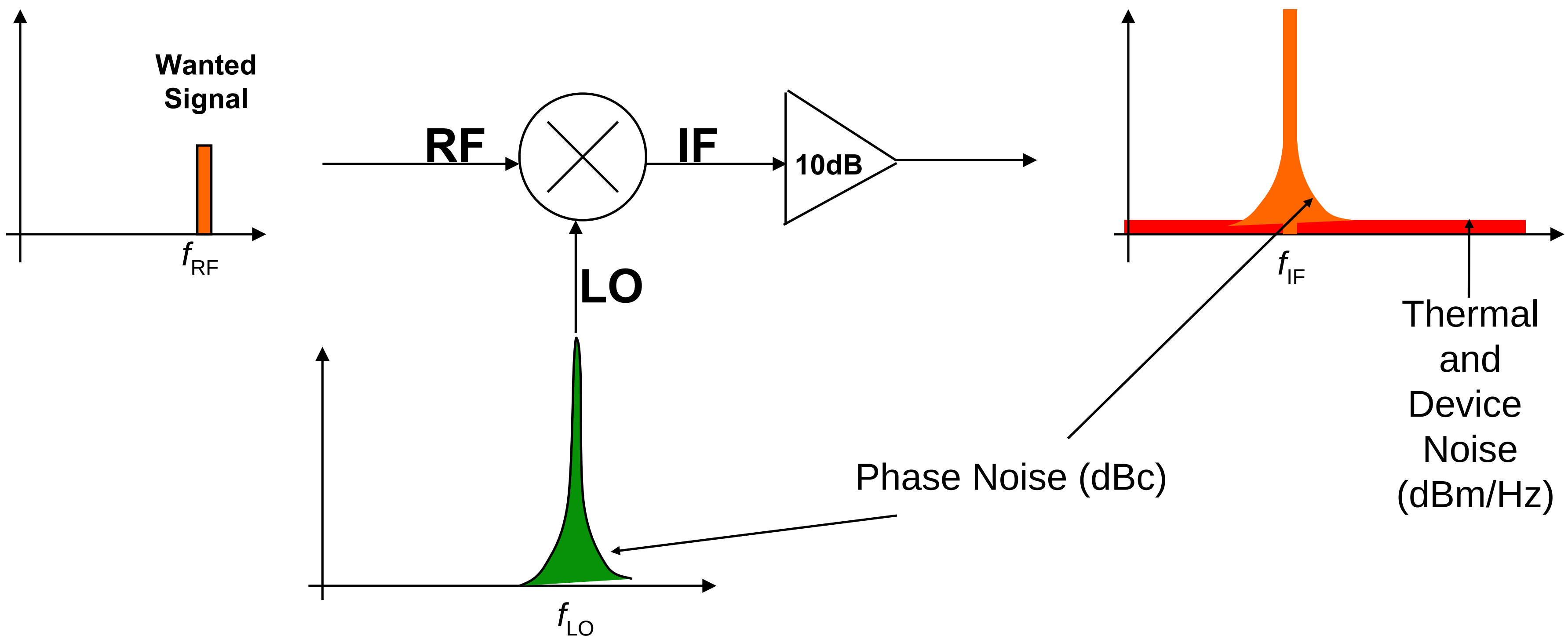
Why is PLL phase noise so important?



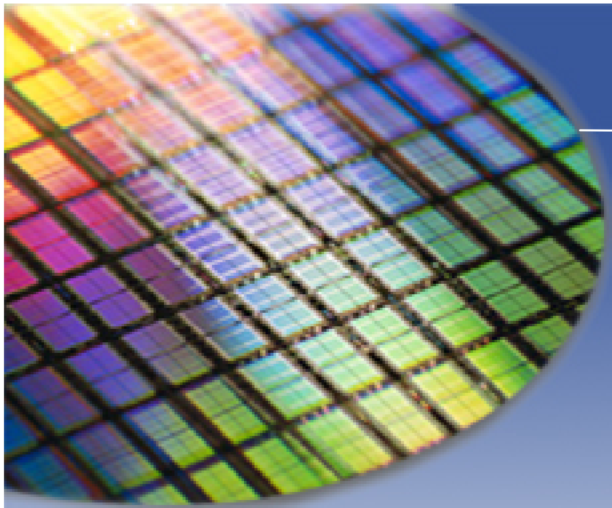
- Reciprocal mixing occurs when the phase noise (side-skirts) of the LO mixes with an unwanted signal and produces an unwanted interference on top of the desired signal

Phase noise vs. Thermal noise

Strong blocker is modulated by phase noise of LO and interferes with desire signal



- **Phase noise "spreads" the desired carrier and is usually specified in dBc/Hz at a particular offset from the LO (usually 1 or 10 KHz)**
- **Background or Thermal noise which is present at all points in the signal chain will be amplified if there is gain in the signal chain.**
- **Amplifier/Mixer Noise Figure will add additional noise to the output of the signal chain (see slide 26). This resulting noise is usually specified in dBm/Hz.**



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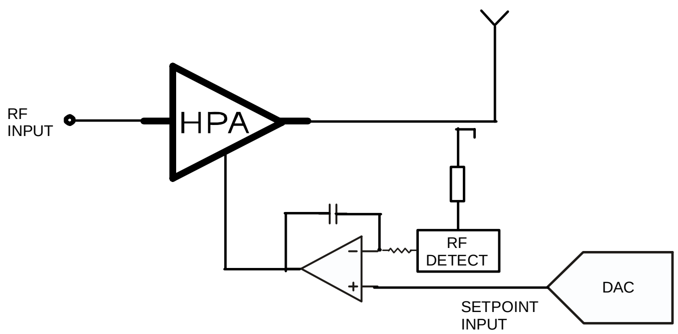
RF Power Detectors

Why measure RF/IF power?

- Thermal Dimensioning (mostly HPA)
- Signal Leveling in receivers (high precision generally not required, usually done at IF)
- Set mobile's power level (RSSI measurement in BTS receiver)
- Prevent interference with other systems and other users in same cell (mobile handset).
- Improve mobile talk time (operate at low end of permissible range, reduce SAR).
- Improve network robustness (operate at high end of permissible range).

Transmit Power Measurement/Control Options



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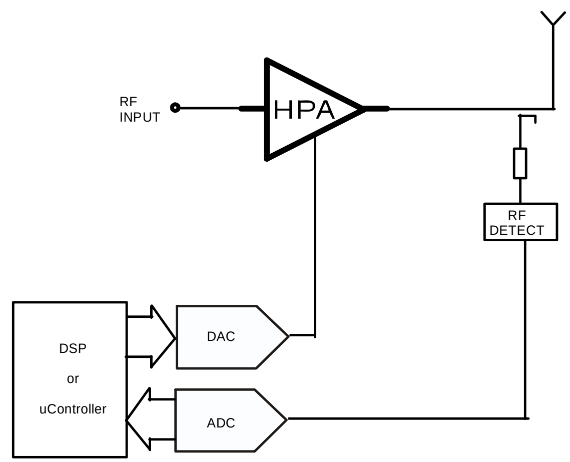

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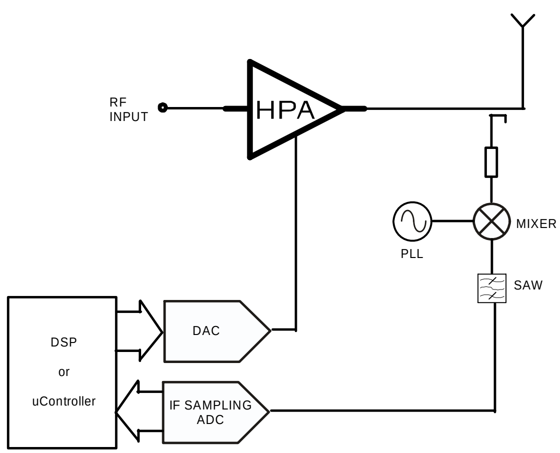

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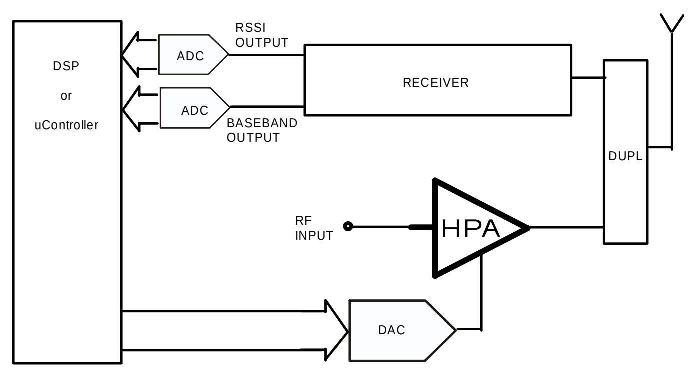
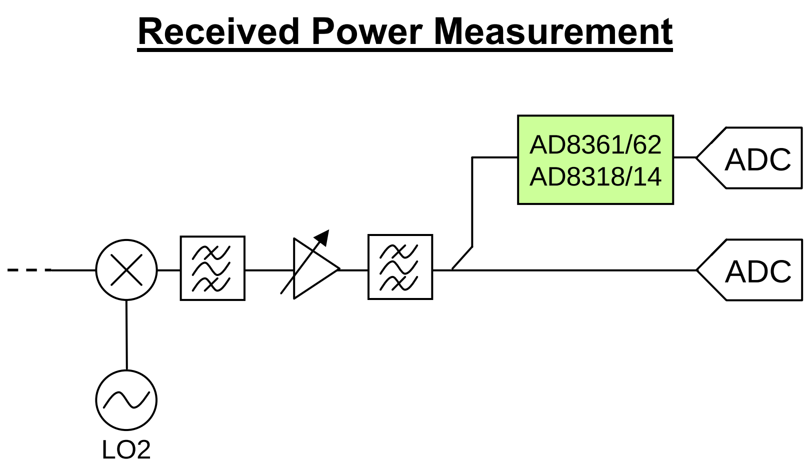
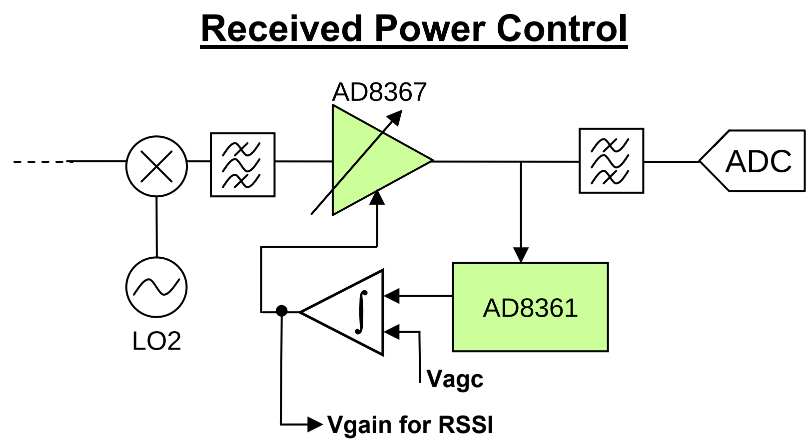


(d)

Receiver Power Measurement/Control Options

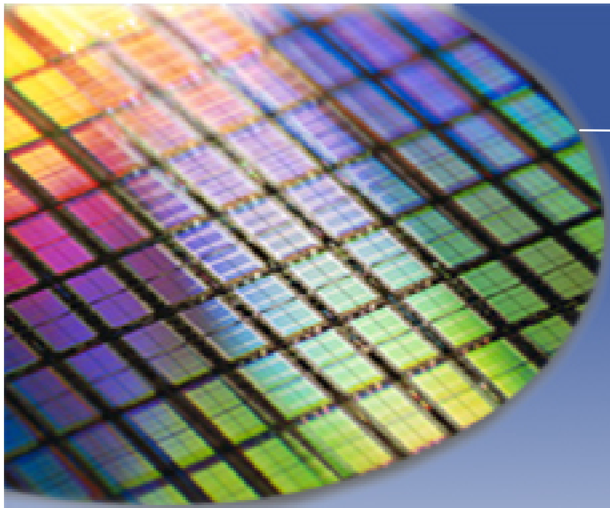




- Measure received power to ensure that the received signal is not too big or not too small when it reaches the end of the signal chain
- Precision requirements for detectors in receivers are generally not as critical as in transmitters

RF Detectors – Critical Specifications

- Linearity and Temperature Stability of Output
- Dynamic Range
- Pulse Response
- Variations due to Power Supply and Frequency Changes
- Ease of Use and Calibration
- Change in response vs. signal crest factor
- Size and overall Component Count



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RF Power Measurement Techniques

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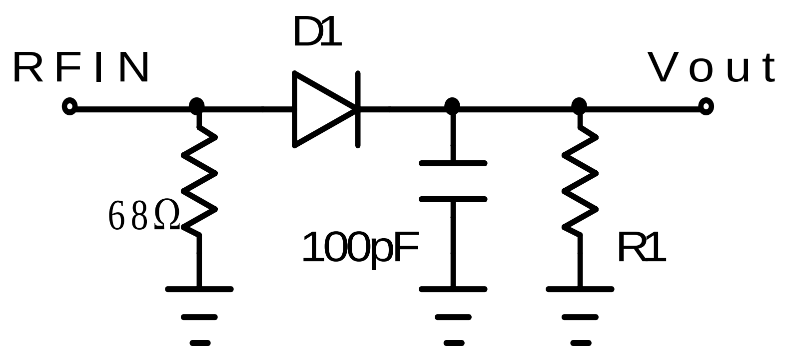
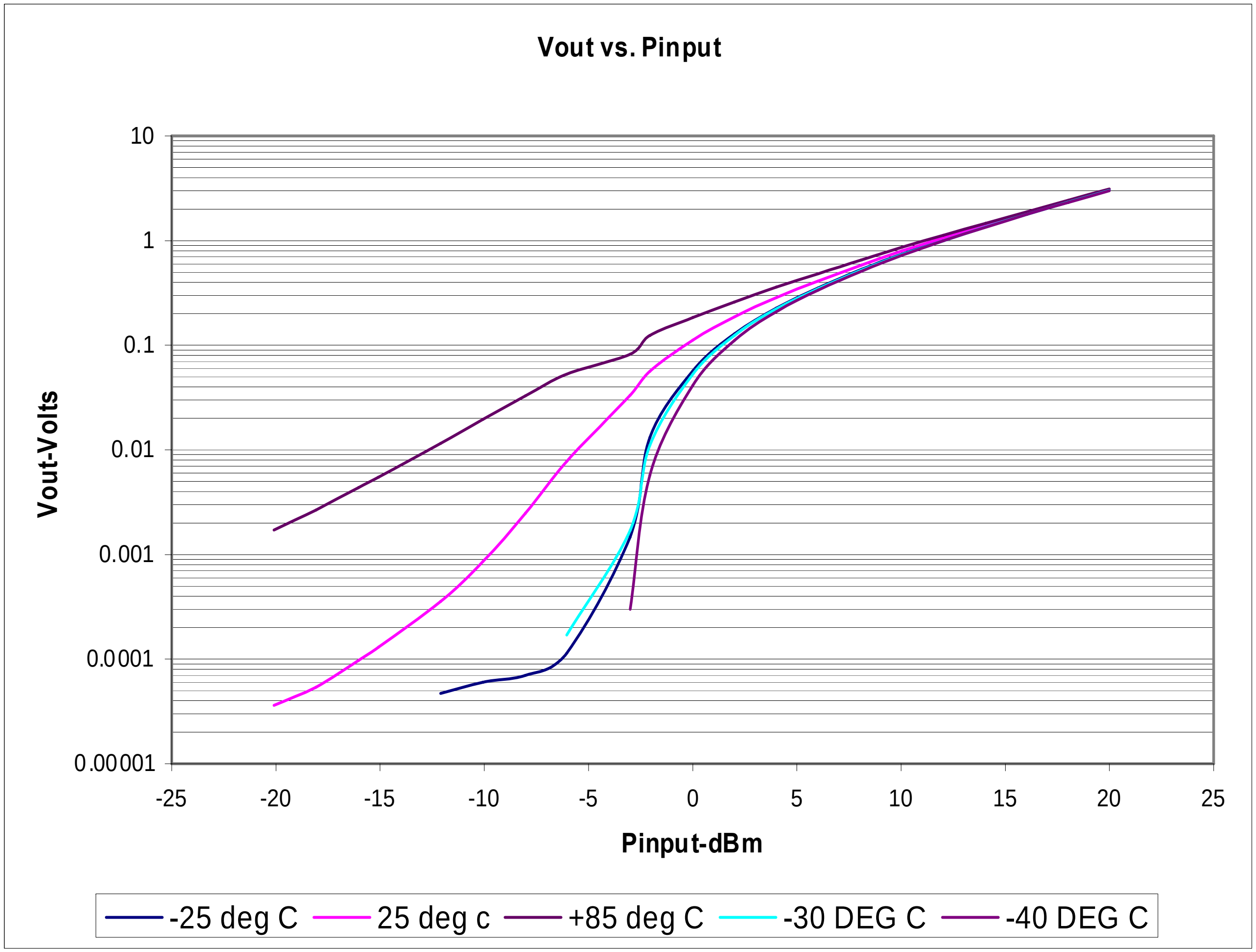
Power Measurement Techniques
Diode Detection

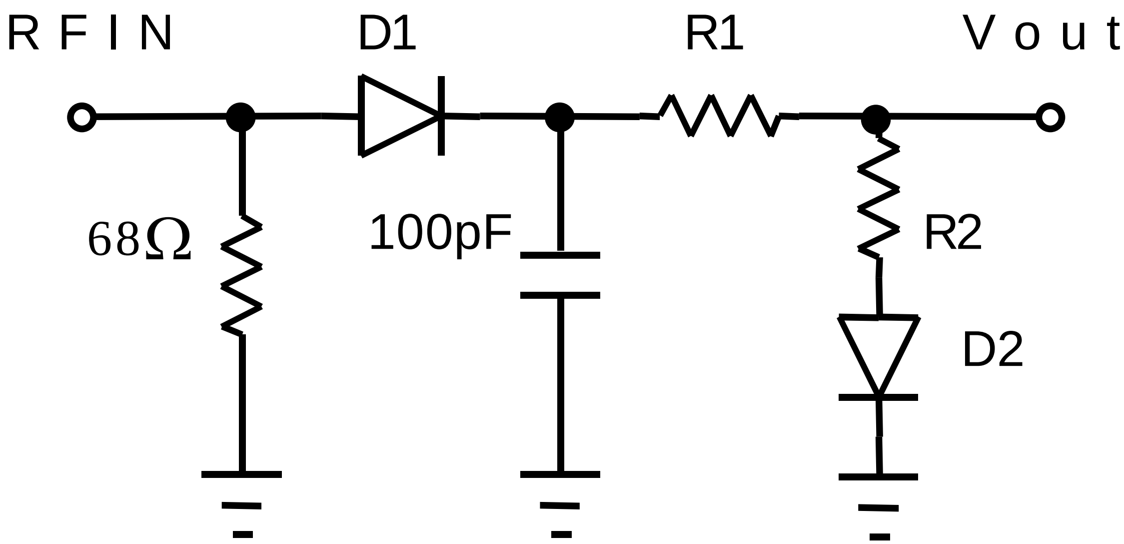


Source: "A Supressed Harmonic Power Detector for Dual Band Phones" Alan Rixon and Raymond Waugh "Applied Microwave and Wireless", November 1999

Transfer Function of Diode Detector

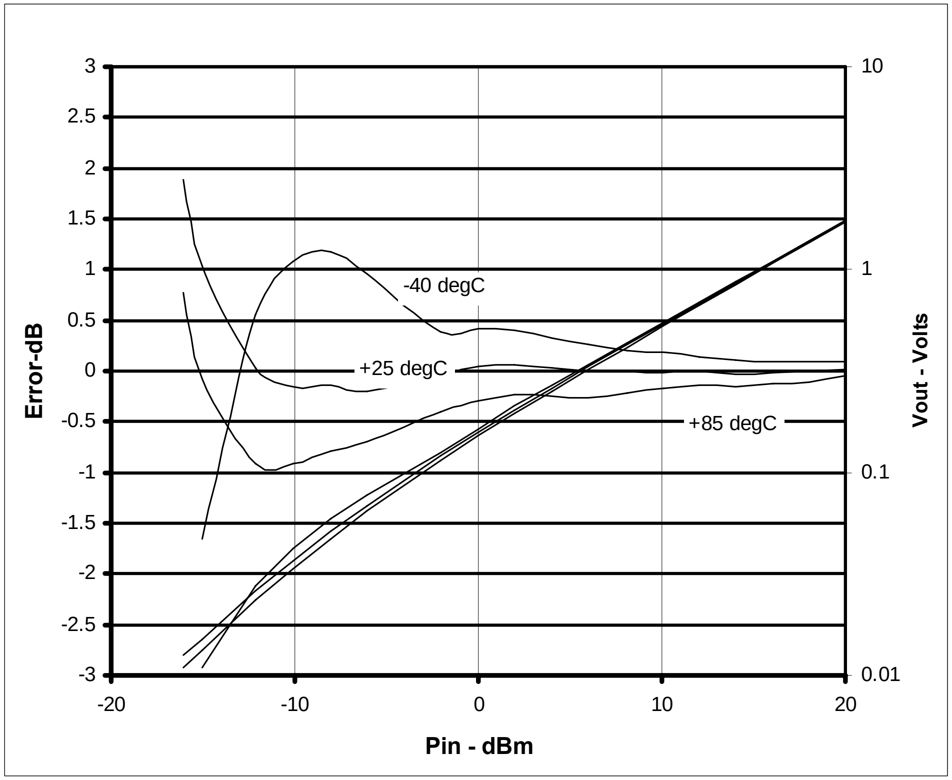


Diode Detector with Temperature Compensation



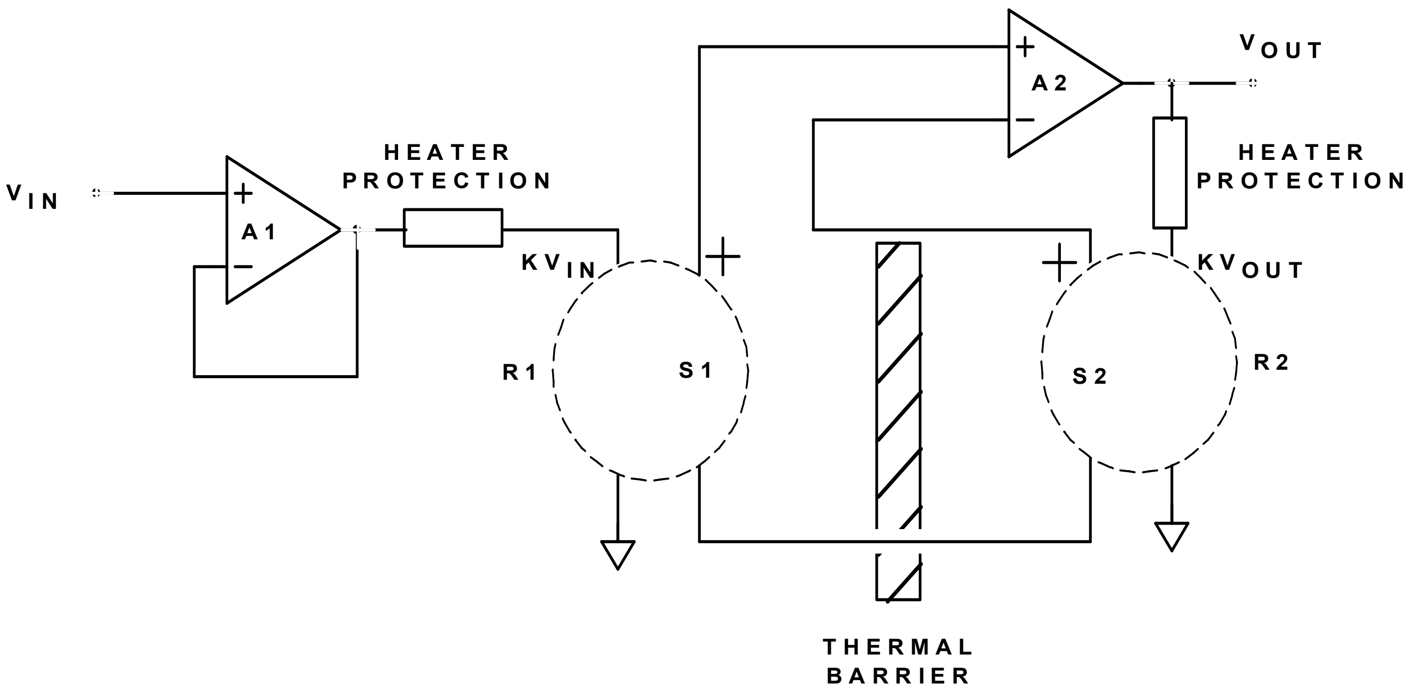
Source: "A Supressed Harmonic Power Detector for Dual Band Phones" Alan Rixon and Raymond Waugh "Applied Microwave and Wireless", November 1999

Transfer Function of Temperature Compensated Diode Detector



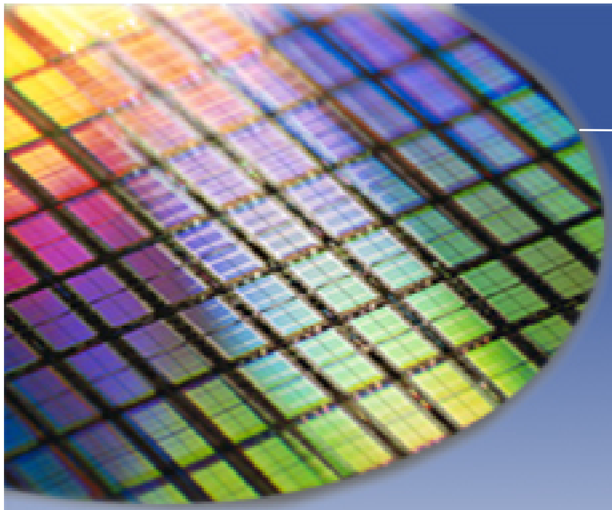
- ***Excellent temperature stability at high power***
- ***Limited Dynamic Range and poor low end temp. stability***
- ***High Resolution ADC required for low end power measurement***
- ***Lots of patented techniques which probably improve this performance***

Thermal Detection



- *Technique is mostly confined to Instrumentation Applications*

ANALOG DEVICES

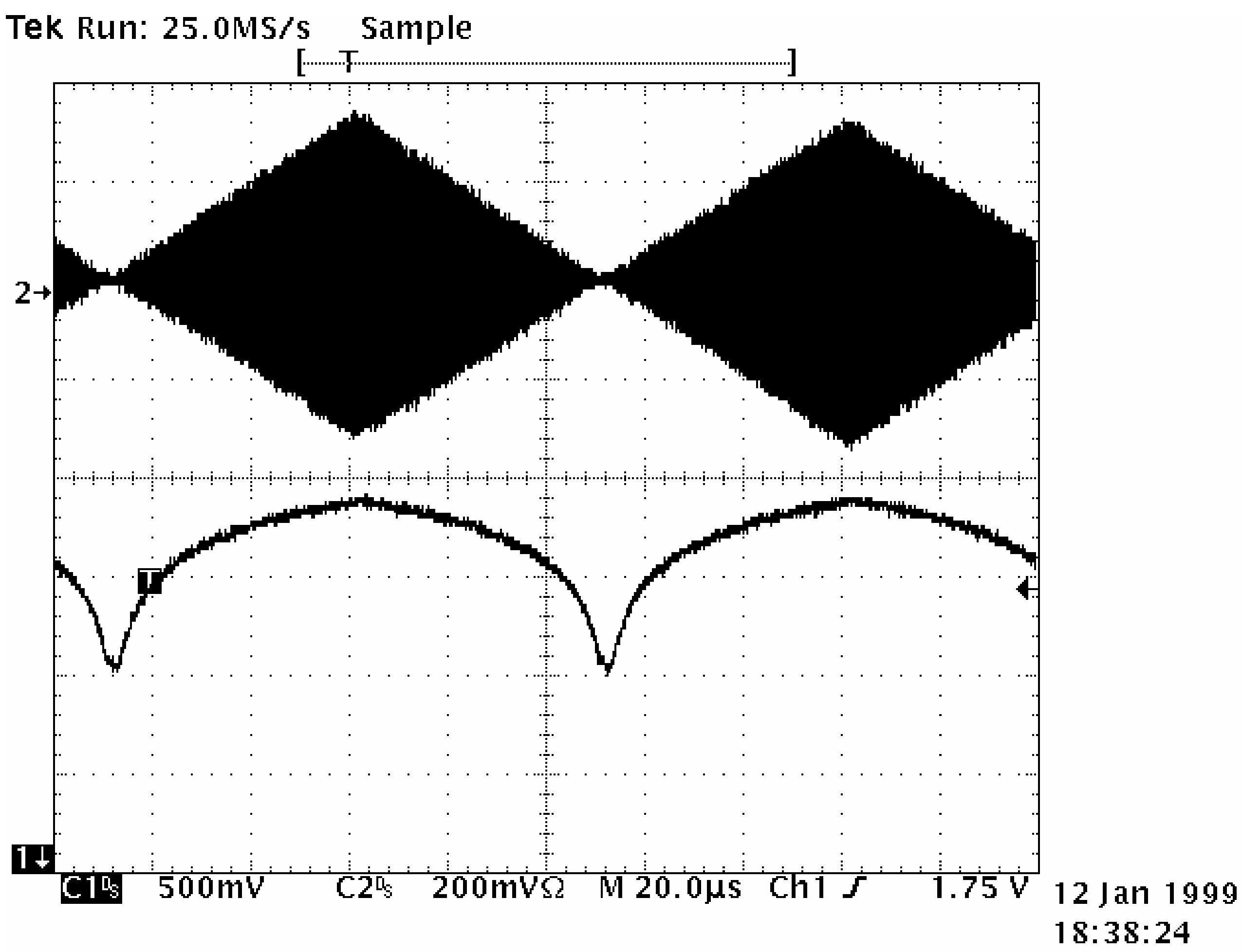


ADI 2006 RF Seminar

Logarithmic Amplifiers

ANALOG DEVICES

Log Amp Transfer Function in Time Domain



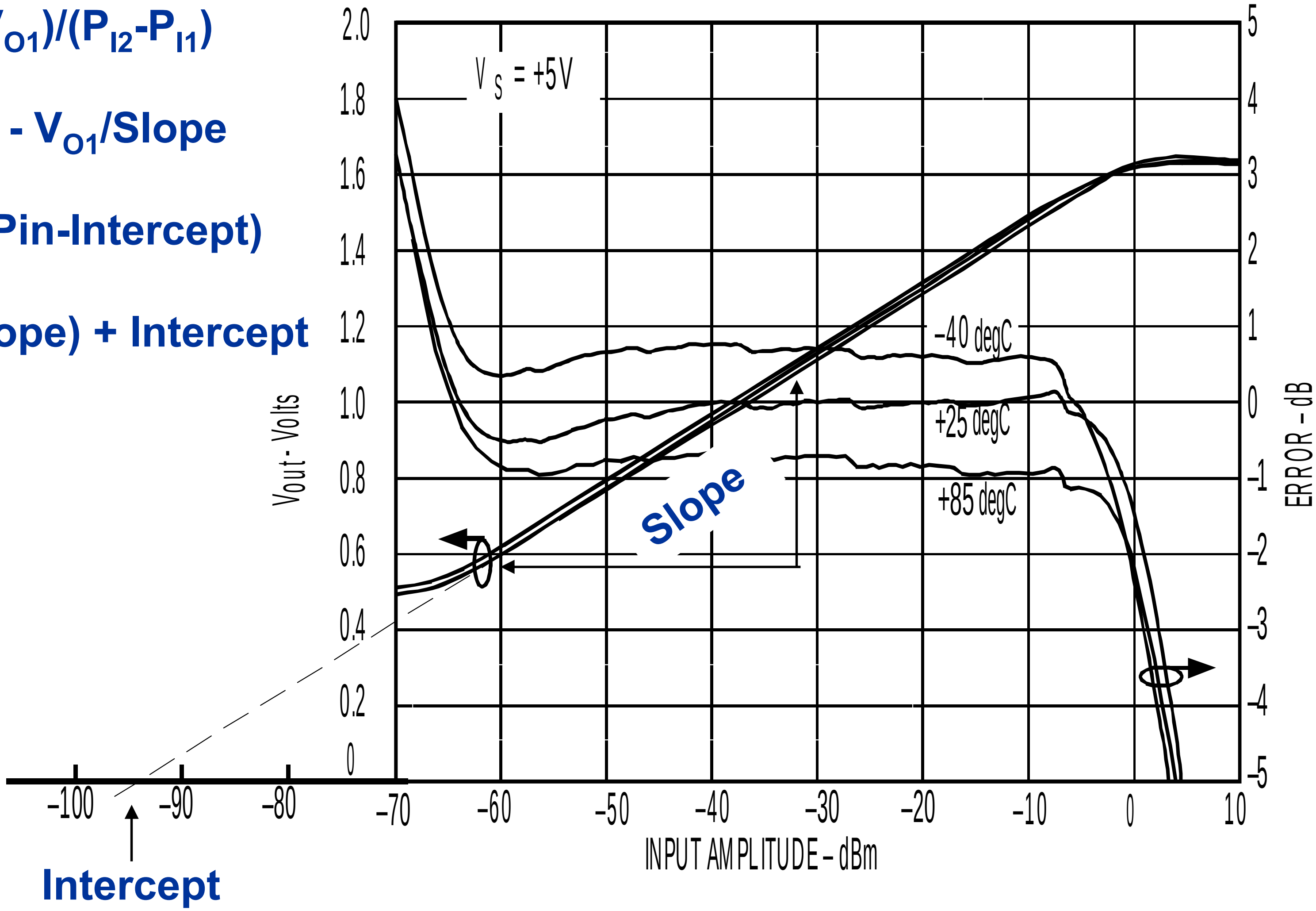
Log Amp Transfer Function - Slope and Intercept

Slope = $(V_{O2}-V_{O1})/(P_{I2}-P_{I1})$

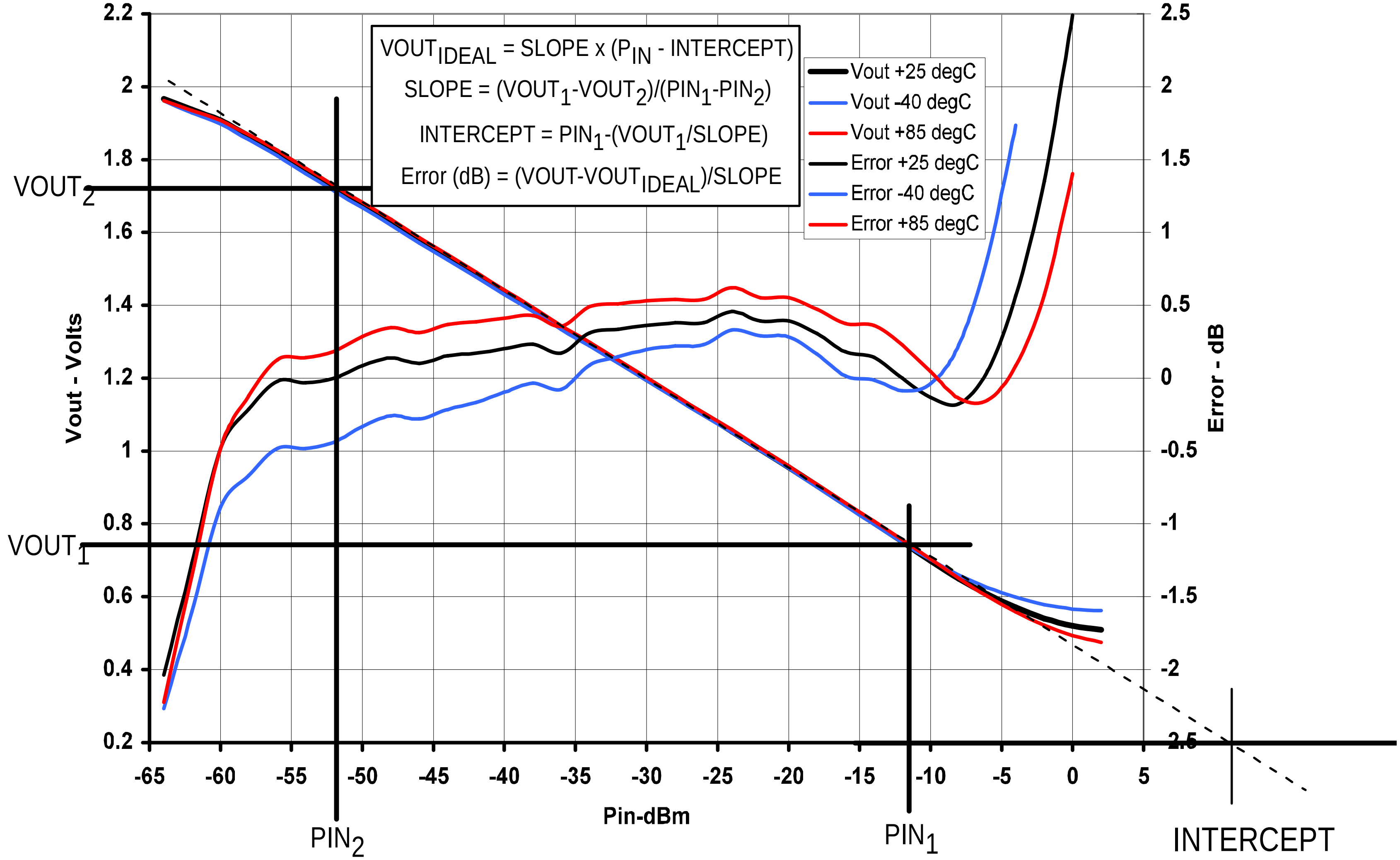
Intercept = $P_{I1} - V_{O1}/\text{Slope}$

Vout = Slope(Pin-Intercept)

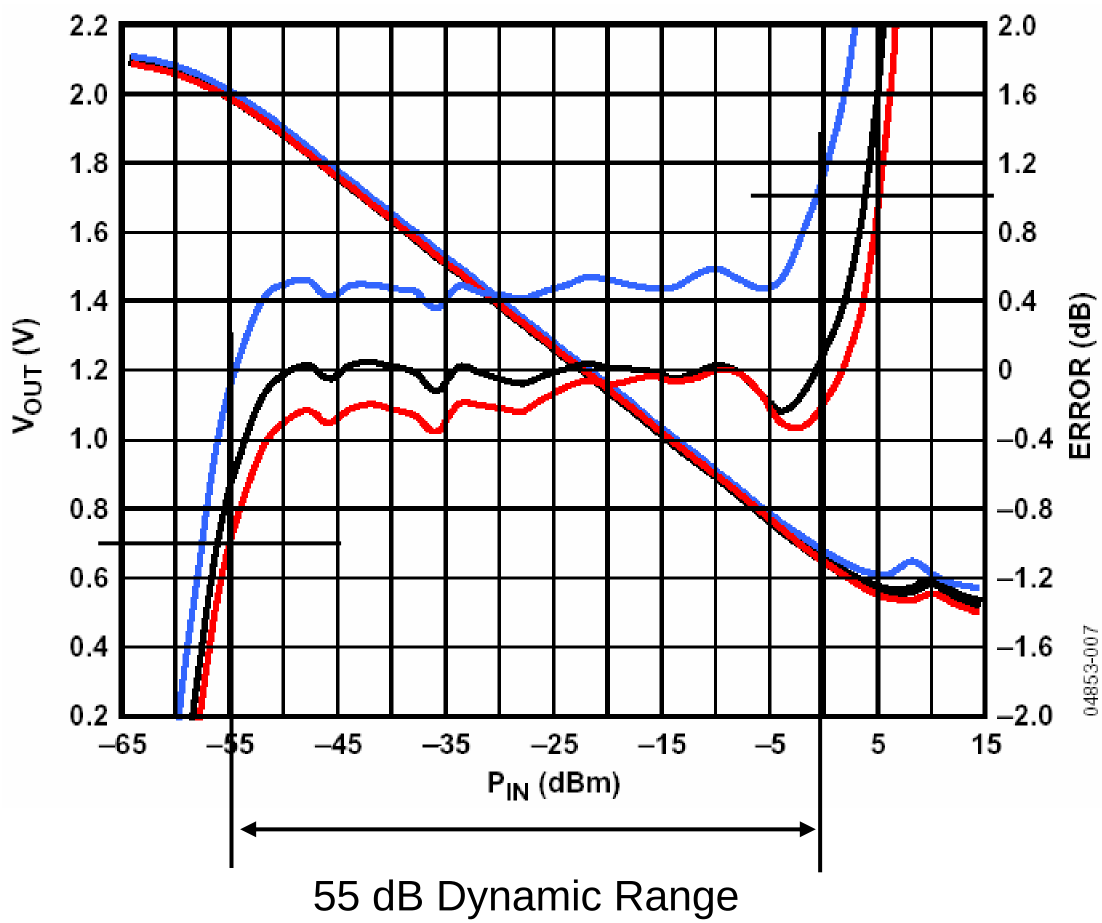
Pin = (Vout/Slope) + Intercept



RF Power Detector Calibration



±1 dB Dynamic Range

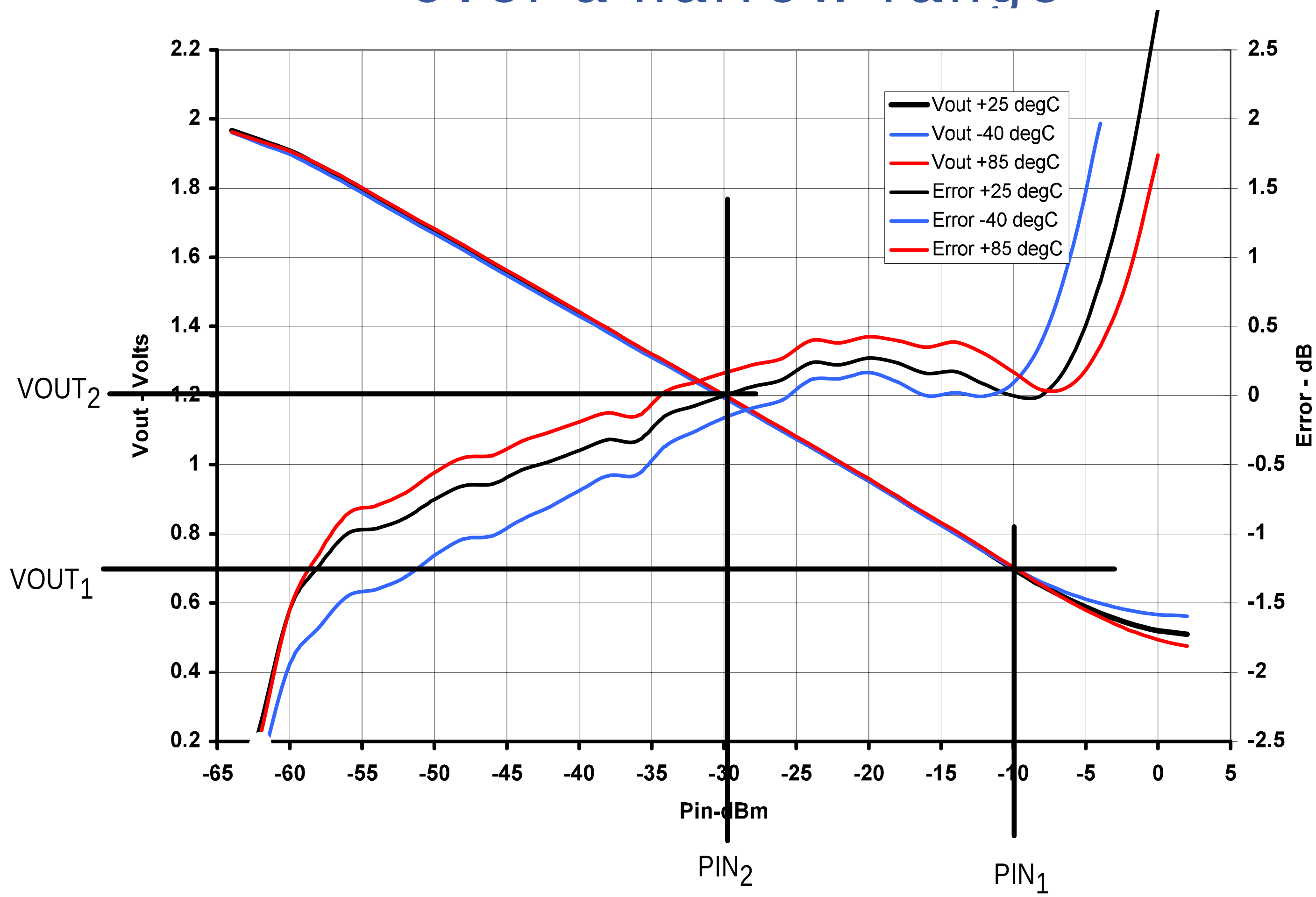


- **Temperature Drift can reduce Dynamic Range**

Detector Calibration Procedure

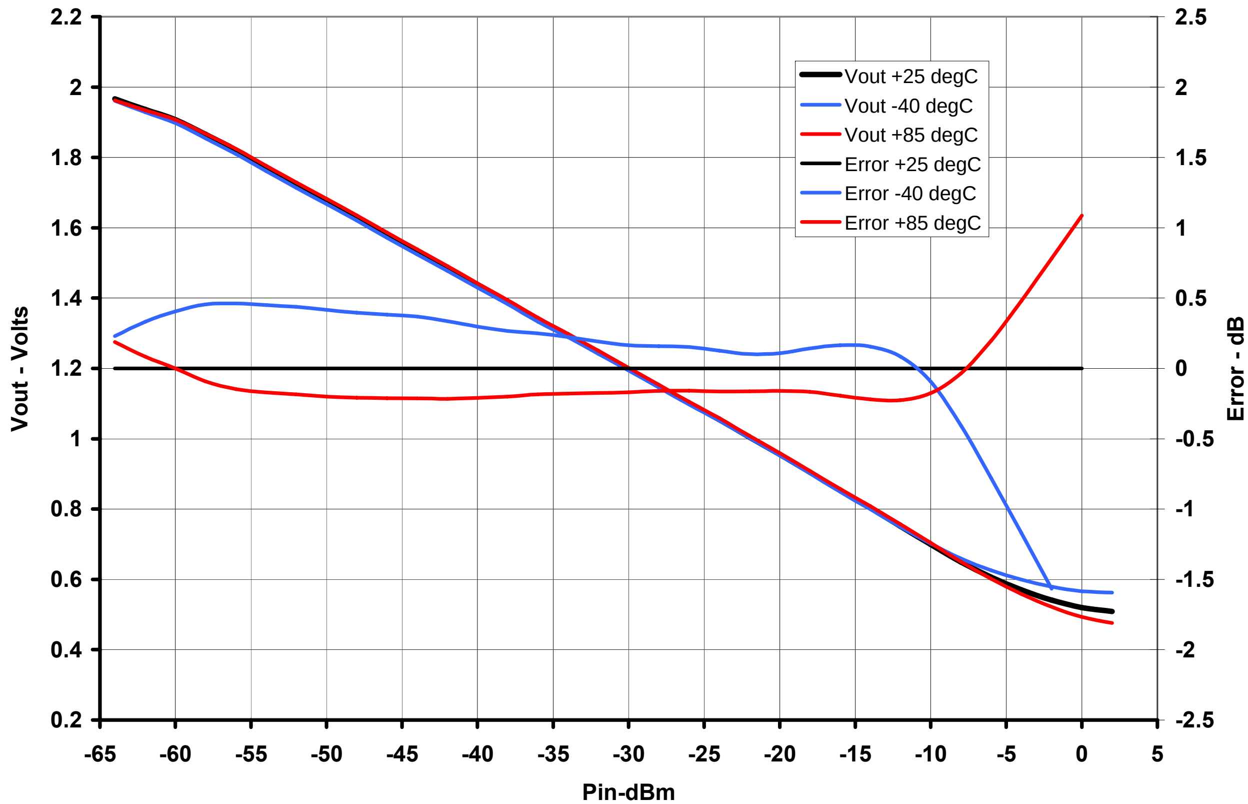
- Factory Calibration: Using a precise power source, measure output voltage from the detector with two known input powers at top and bottom of desired input range
- Perform calibration measurements only at room temperature
- Calculate SLOPE and INTERCEPT and store in non-volatile memory
- When equipment is in operation measure detector output voltage using ADC
- Calculate power using "Pin = (Vout/Slope) + Intercept"
- No temperature compensation necessary

Adjust Calibration Points for optimal accuracy over a narrow range



- Calibrate for highest accuracy at max RF power and degraded accuracy at lower powers

Temperature drift vs. Output Voltage at 25ºC



- Calibration eliminates error due to non-linearity at 25 ºC

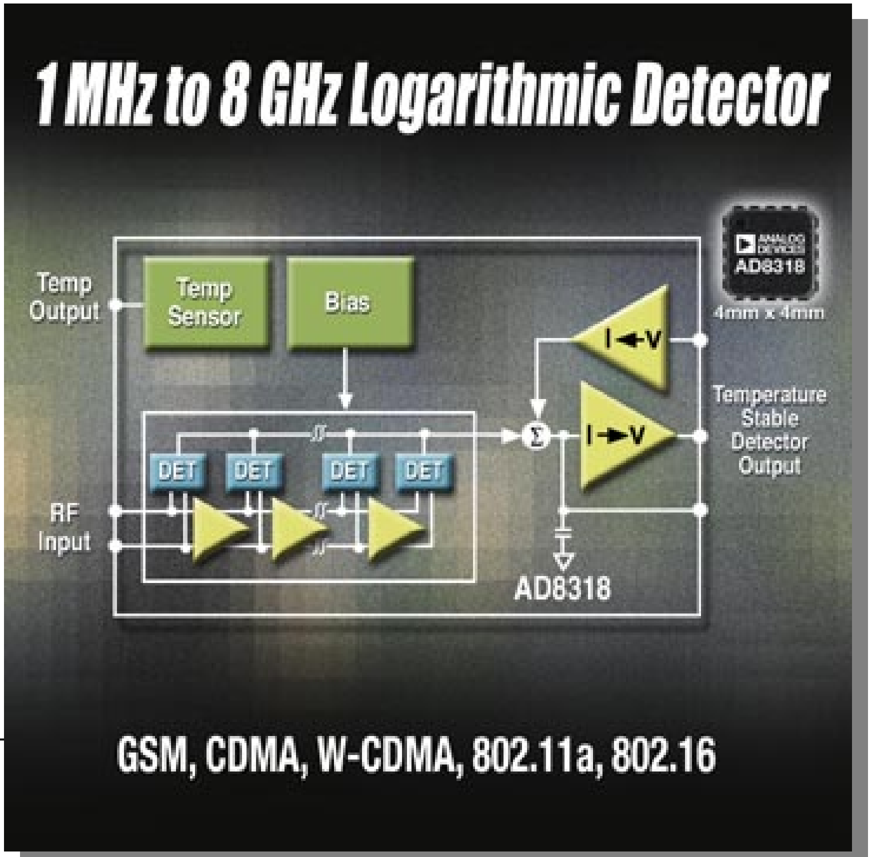
Temperature drift vs. Output Voltage at 25ºC

- *Removes error due to non-linearity at 25ºC*
- *Provides larger dynamic range and improved accuracy*
- *Method however does not account for non-linearity in the transfer function at room temperature*
- *For practical implementation, calibration measurements must be taken at multiple input powers (multi-point calibration vs. 2-point calibration)*

AD8318: Highest Performance Log Amp

KEY SPECIFICATIONS

- ❑ **Bandwidth 1MHz to 8Ghz**
- ❑ ***Stability over temperature: ±0.5 dB***
- ❑ **Pulse response time 10 ns**
- ❑ **Package: 4mm×4mm, 16-pin LFCSP**

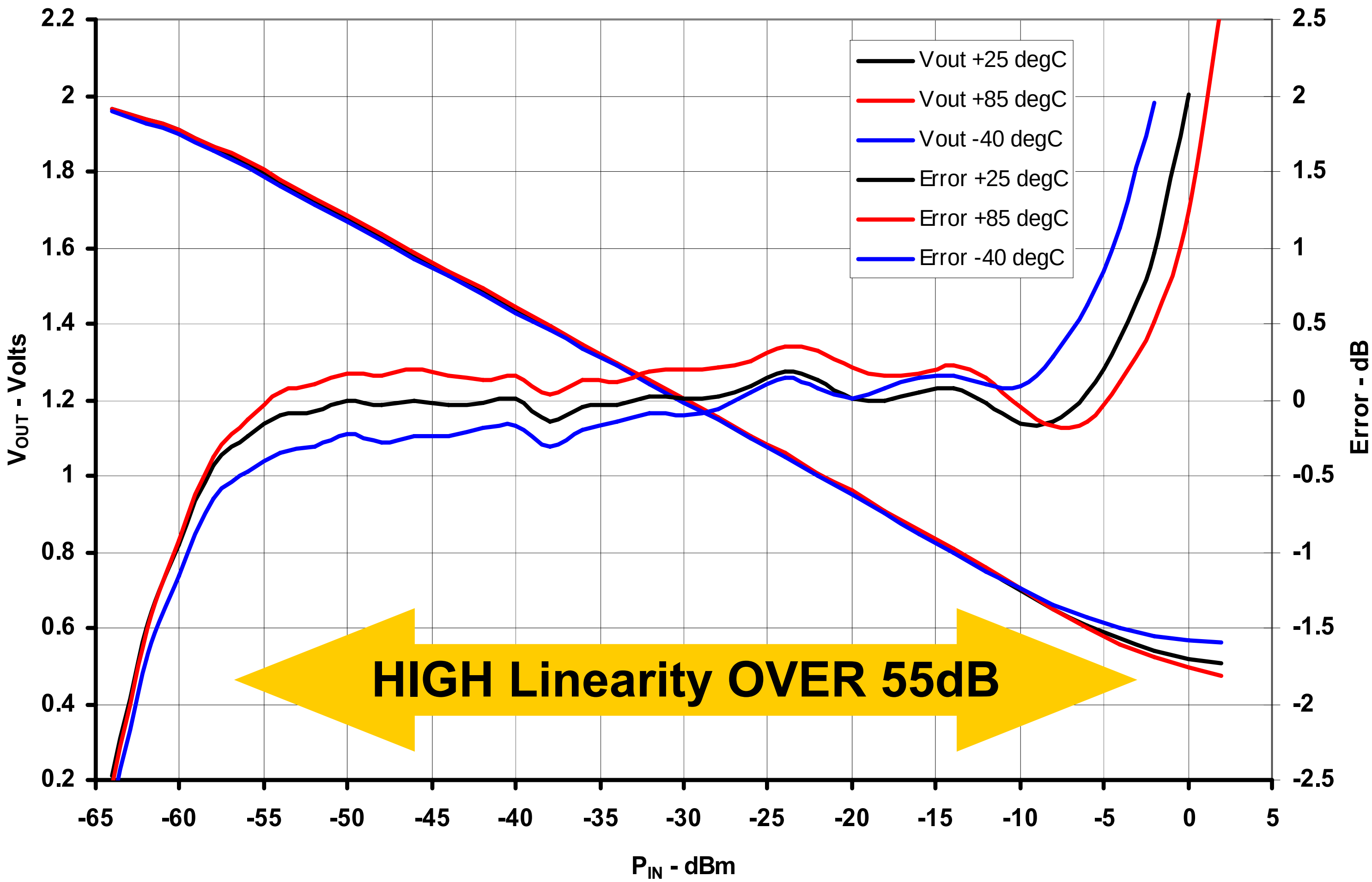


FEATURES

- ❑ **Integrated temperature sensor**
- ❑ **Low noise measurement/controller output VOUT**
- ❑ **Power-down feature: <1.5 mW at 5 V**
- ❑ **Fabricated using high speed SiGe process**

AD8318 High Performance Log Amp

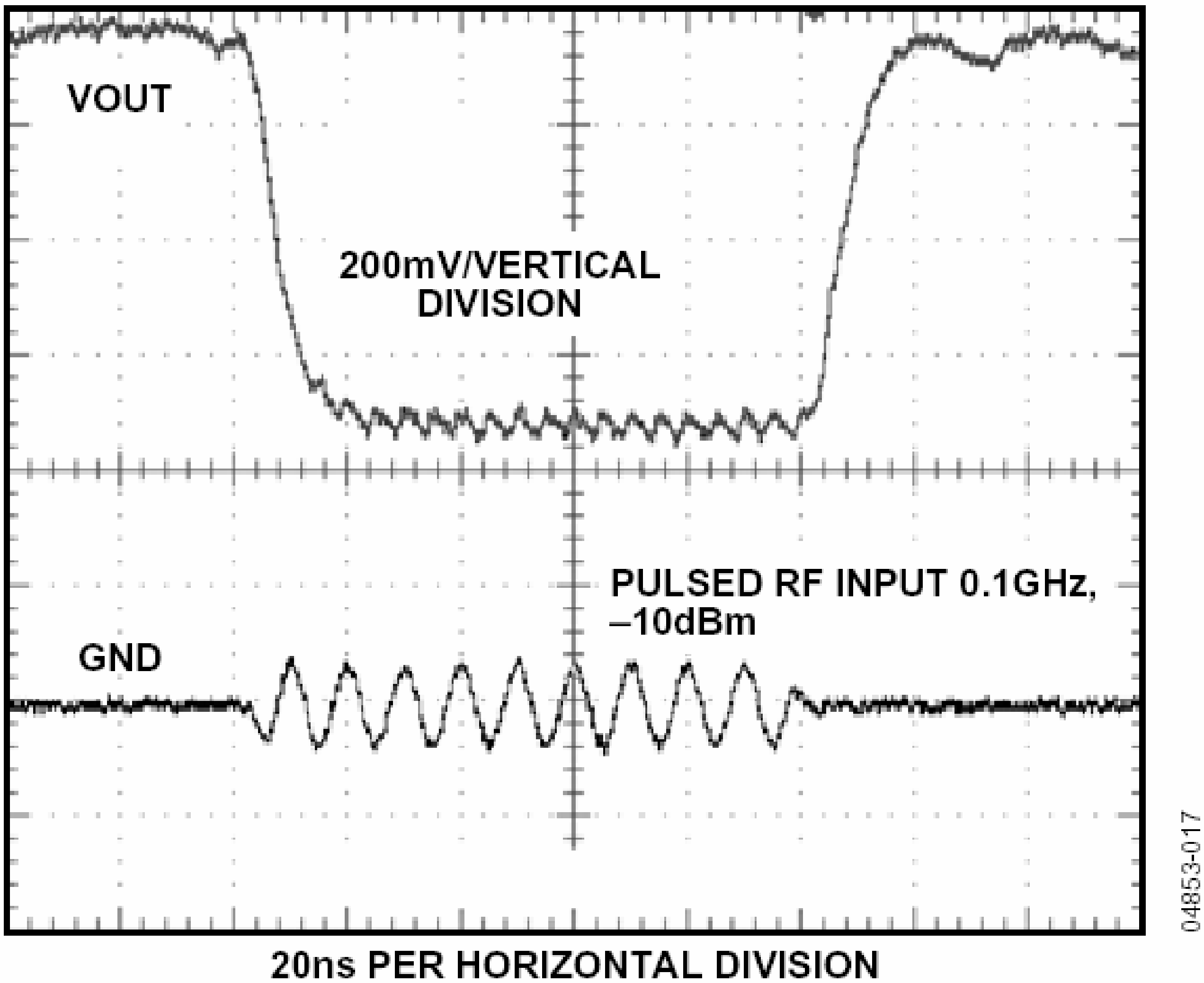
< ±0.5 dB accuracy over temperature



5.8 GHz

Log Amp Pulse Response Time

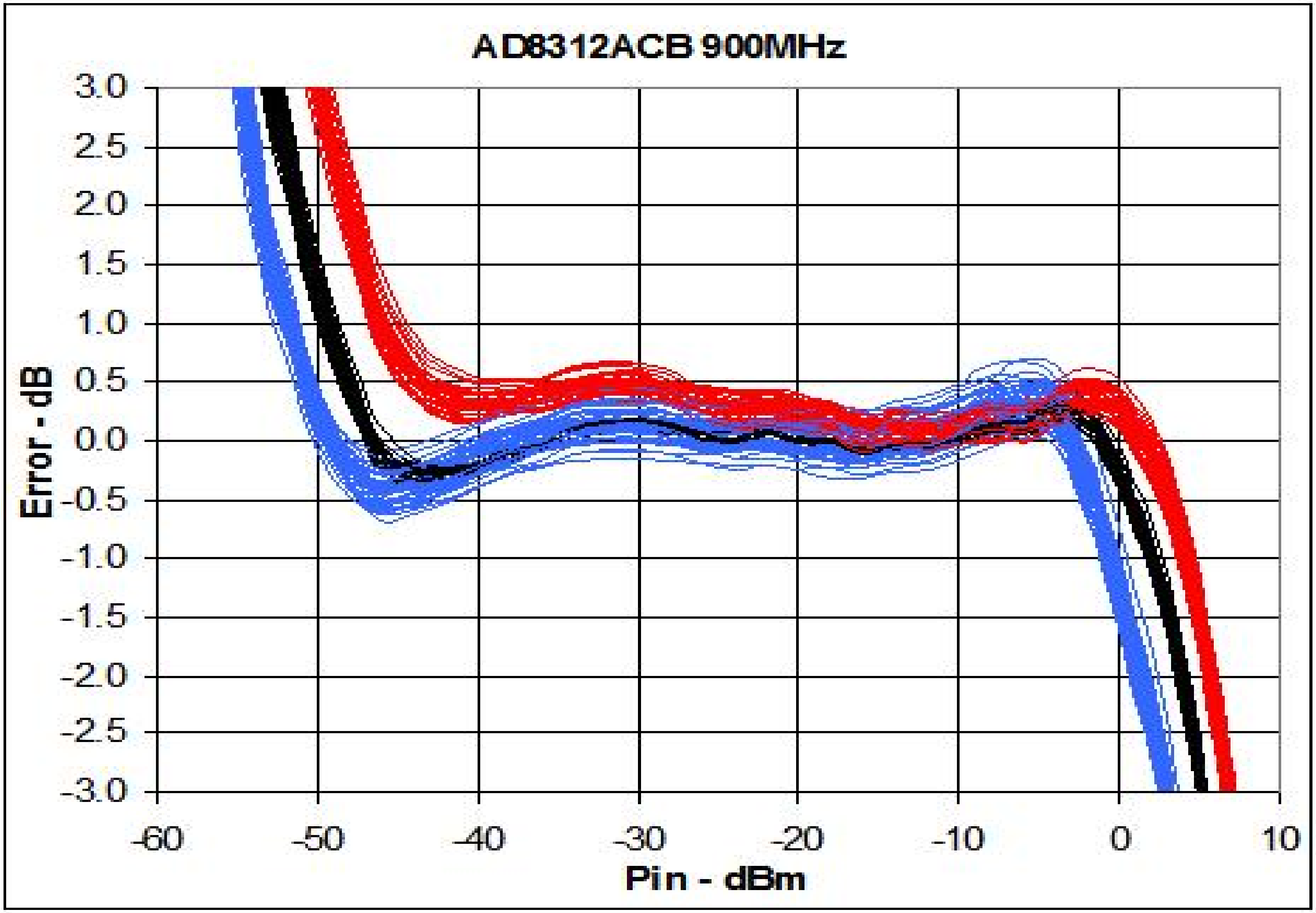
10ns Response Time (10% - 90%)



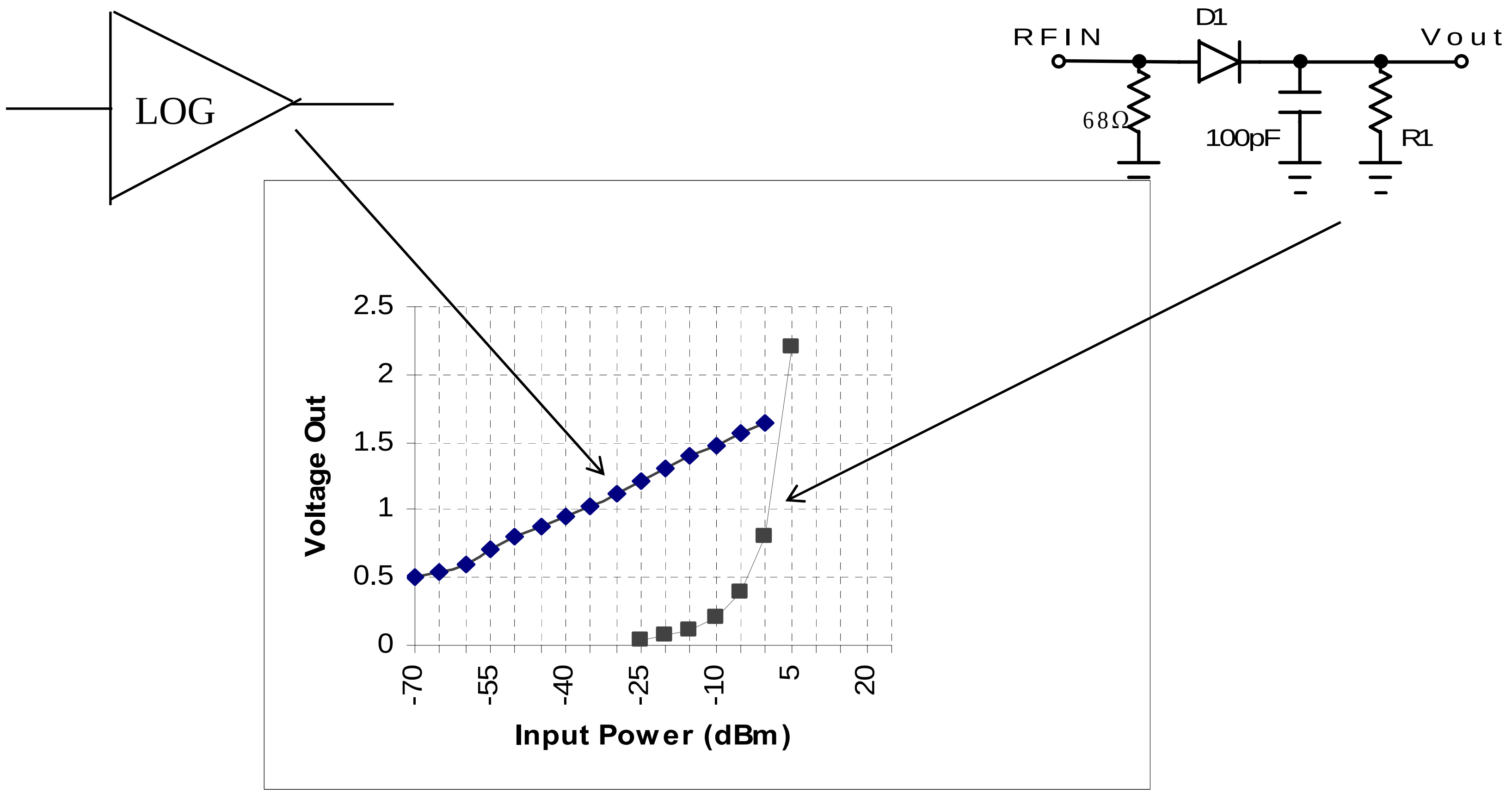
Typical and Maximum Errors vs. Temperature

- Production testing of drift over temperature is generally not economical for IC manufacture (or for end equipment manufacture)
- Guaranteed-not-Tested (GNT) specs rely too much on statistics and are much too conservative
- Solution: Show performance data from multiple devices drawn from multiple factory lots

Typical and Maximum Errors vs. Temperature



Log Amp Detectors vs. Diode Detectors



Log Amp Detectors vs. Diode Detectors

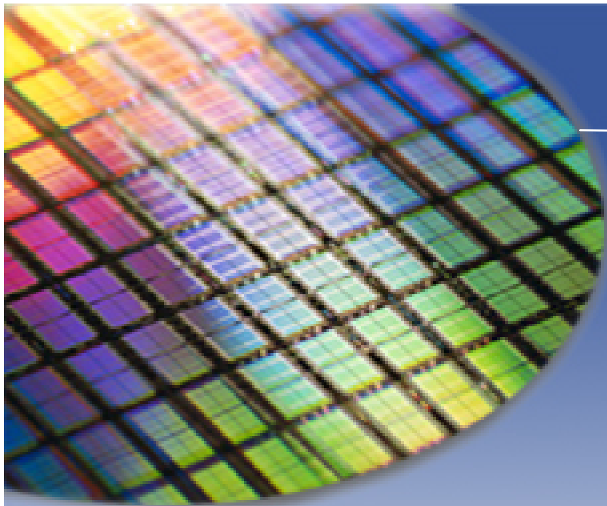
- Log Amps have a higher dynamic range (40 dB or greater vs. 20-30 dB for a diode detector)
- Log Amps provide good temperature stability over a wide dynamic range.
- Diode detectors only provide good temperature stability at max input power (typically +15 dBm)

Log Amp Detectors

Part No.	*RF Freq (MHz)*	*Dynamic Range (dB)*	*Temp Drift (dB)*	Response Time (ns)	Package	Comments
AD8309	*5 to 500*	*100*	*±1*	67	16-lead TSSOP	Amplitude and Limiter Outputs
AD8310	*dc to 440*	*95*	*±1*	15	8-lead MSOP	
AD8318	*1 to 8000*	*60*	*±0.5*	8	16-LEAD 3x3 mm CSP	
AD8317	*1 to 10000*	*50*	*±0.5*	5	8-LEAD 3x2 mm CSP	
AD8319	*1 to 10000*	*40*	*±0.5*	5	8-LEAD 3x2 mm CSP	
AD8302	*LF to 2700*	*60*	*±1*	50	14-LEAD TSSOP	Dual Gain and Phase Detection
ADL5519	*1 to 10000*	*50*	*±0.5*	8	24-LEAD LFCSP	Dual Power and Gain Detection

Log Amps - Summary

- Provide power detection over large dynamic range (up to 100 dB)
- Operation from DC to 10 GHz
- With 2-Point Calibration, measurement accuracy of << ±1 dB is achievable.
- Devices are generally configured to provide a broadband 50 Ω match
- Pulse Response times of <10 ns are achievable.
- Power consumption varies from 5 mA to 70 mA

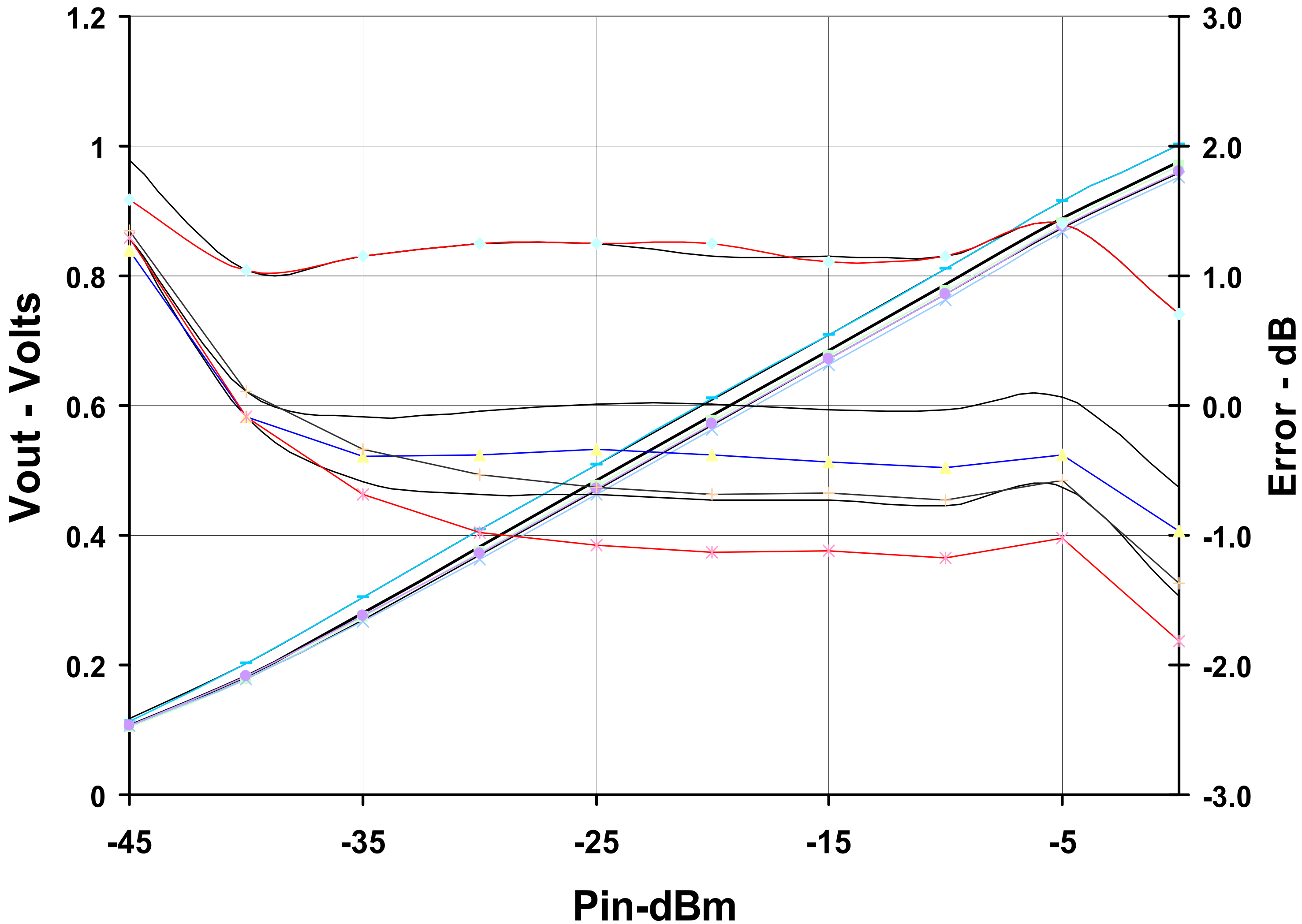


ADI 2006 RF Seminar

RMS-Responding RF Detectors

ANALOG DEVICES

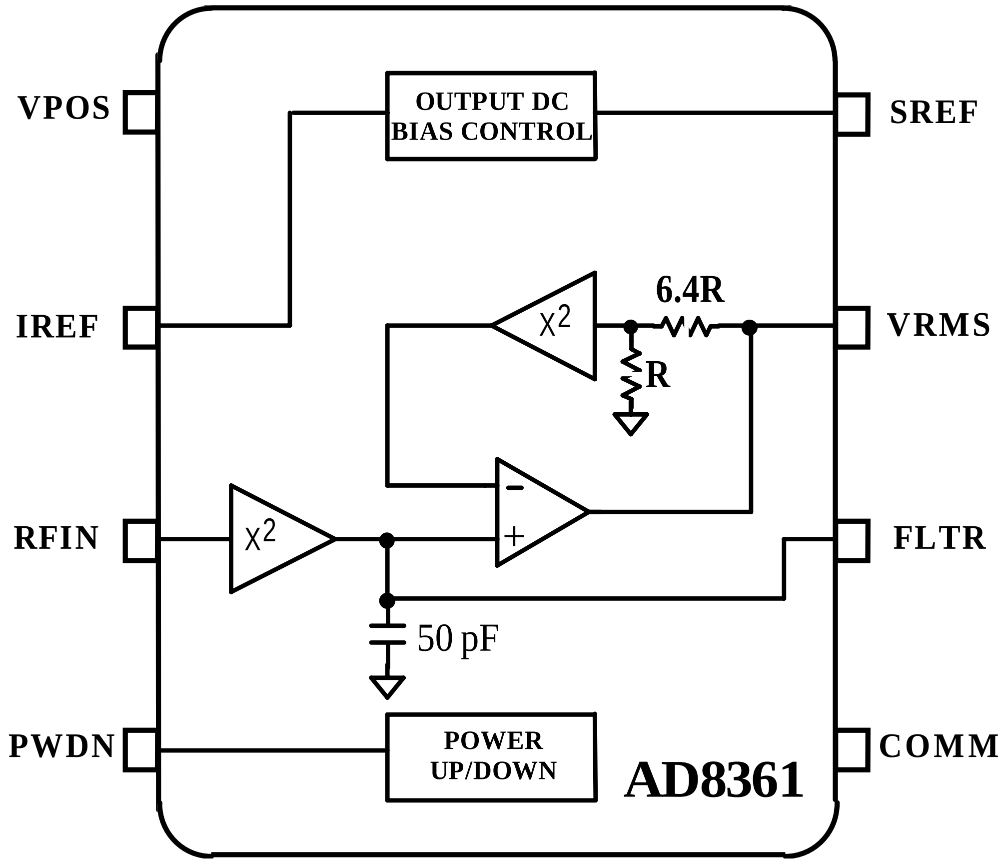
Response of a Successive Detection Log Amp to Varying Signals with Various Crest Factors



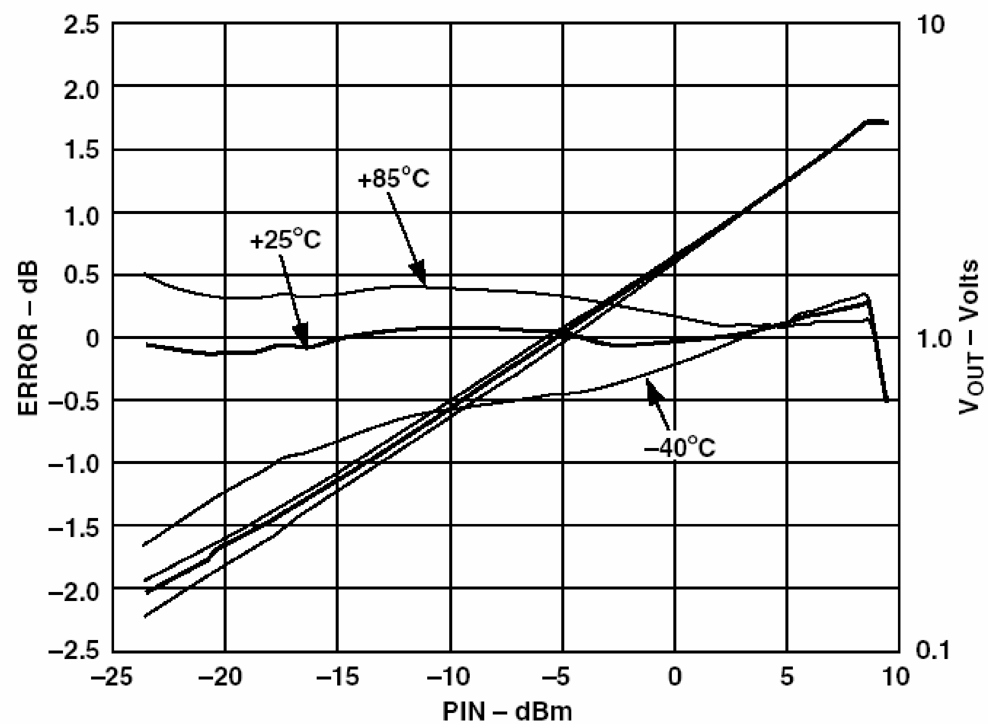
Using a Successive Detection Log Amp to Measure Signals with Varying Crest Factors

- Successive Detection Log Amps produce varying output voltages with varying crest factors
- Intercept varies but slope is unaffected
- Not an issue in systems with constant crest factor
- If the system knows which signal types are being transmitted, a correction factor (from a look-up table) can be applied.
- If the crest factor of the signal is unknown, an RMS-responding detector must be used.

An RMS-Responding RF Detector



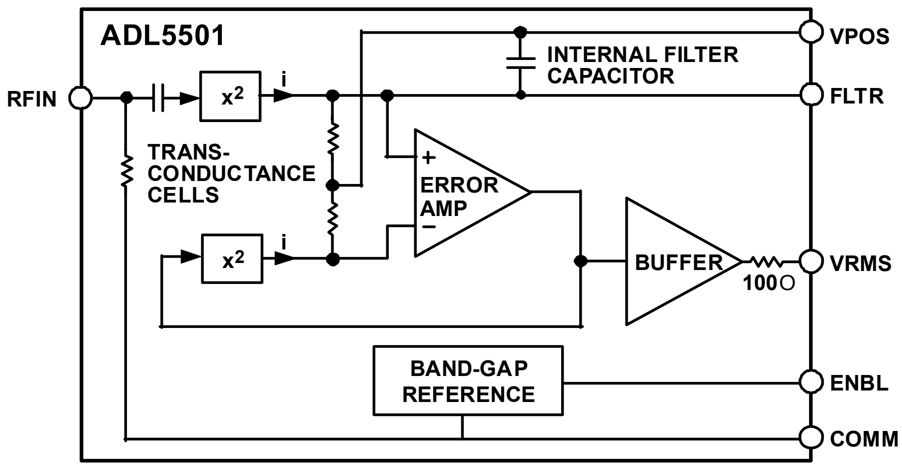
Transfer Function and Temperature Drift of AD8361 RMS-To-DC Converter



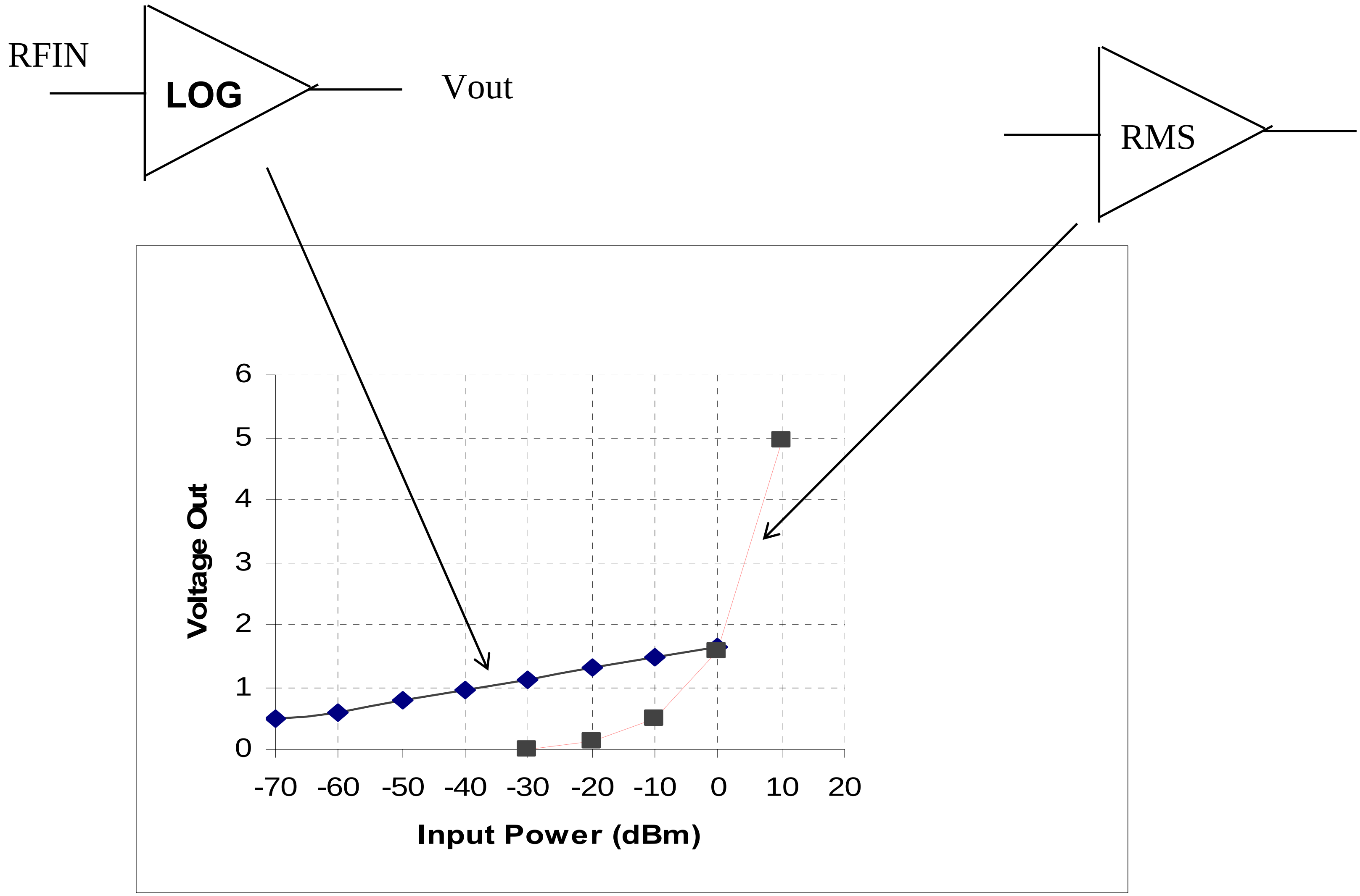
- ❑Output Voltage increases exponentially as input increases in dB (i.e. response is linear in V/V, not logarithmic
- ❑Device achieves best temperature stability at max power (desirable for most applications)

ADL5501 RMS / TruPwr Detector

- Linear in Volts
- +/- 0.25dB accuracy and temperature stability
- +/- 0.1dB accuracy and temperature stability at the top end of the input power range where it counts most.
- 100 MHz to 4.0GHz
- SC-70 Package
- Ideal for Measuring Complex Waveforms with varying crest factors (WCDMA, HSDPA, HSUPA, CDMA2000, TD-SCDMA, WiMax).

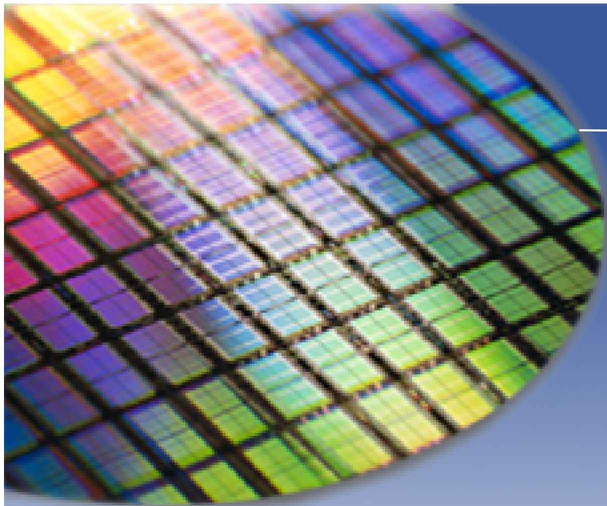


Log Amps vs. Low Range RMS-to-DC Detector



Log Amps vs. Low Range RMS-to-DC Detector

- Log Amps have higher dynamic range but rms-to-dc converters have more resolution at the high end. Measurement precision is often most critical at high output power (Emissions Regulations, SAR, etc.)
- Log Amps consume constant supply current independent of input level. RMS-to-DC converters supply current increases with input signal power.

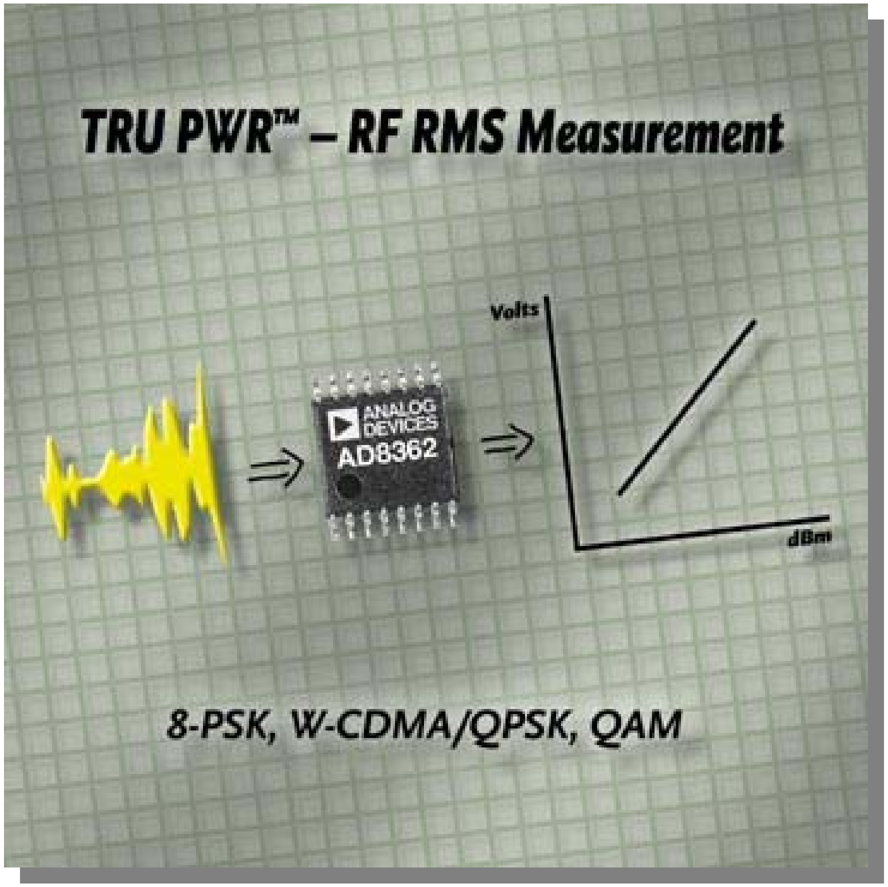


High Dynamic Range RMS Detection

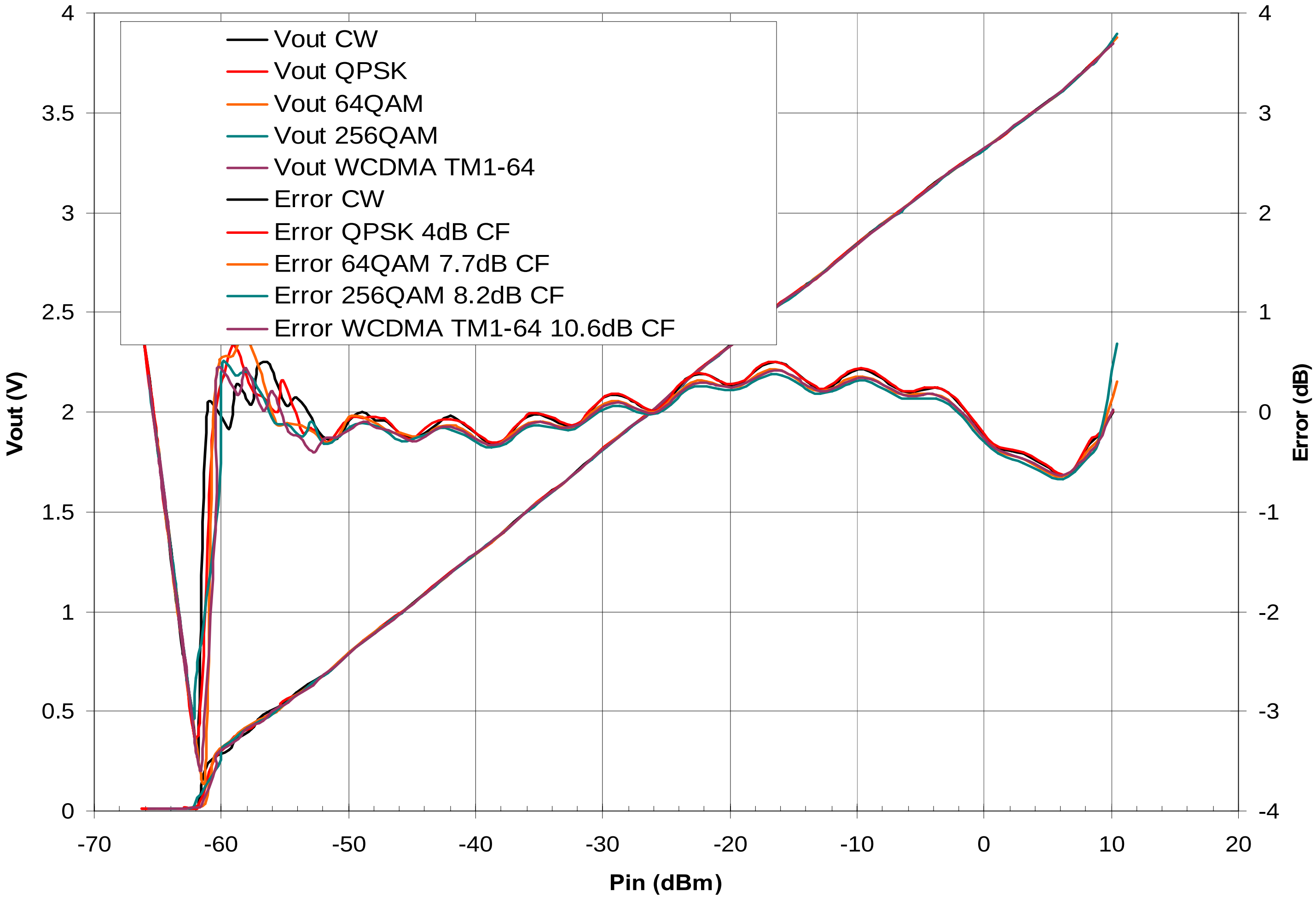
AD8362 60 dB TruPwr ™ RMS Detector

KEY SPECIFICATIONS
- Dynamic Range: >60dB
- Temperature Stability: +/-1dB
- Frequency Range: LF to 2.7GHz
- Package: 16 Lead TSSOP

FEATURES
- True RMS responding power detector
- Waveform and Modulation Independent
- Linear-in-dB output



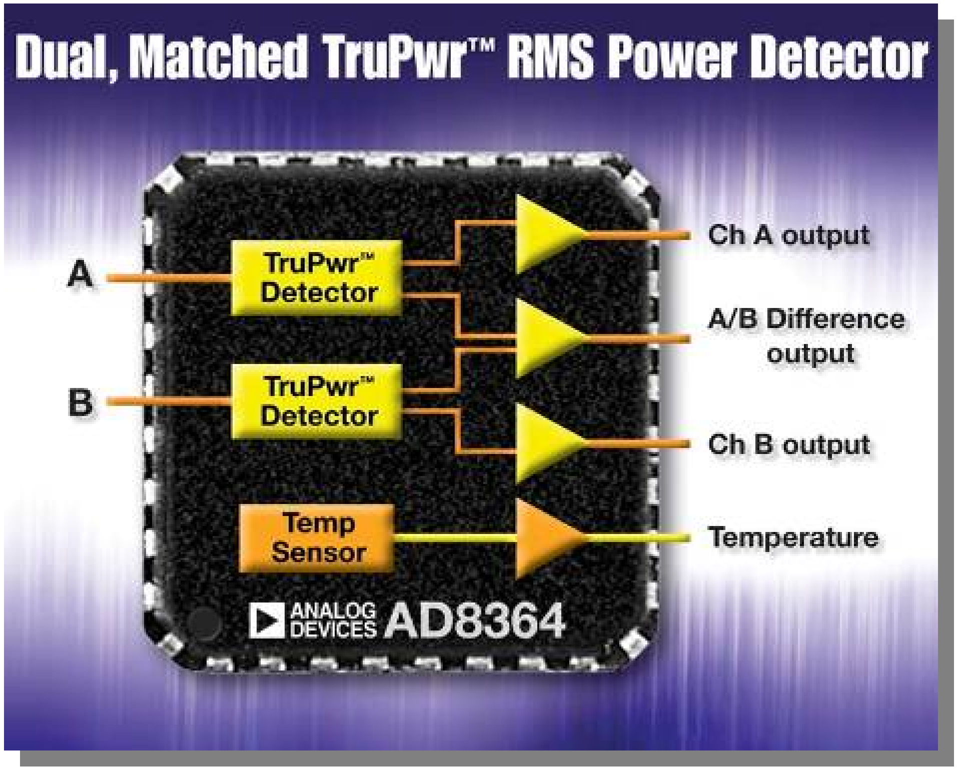
Response of AD8362 RMS Detector to CW, QPSK and QAM Signals



@1.9 GHz, Vtgt = 0.625 V

ANALOG DEVICES

AD8364 Dual Channel TruPwr ™ Detector



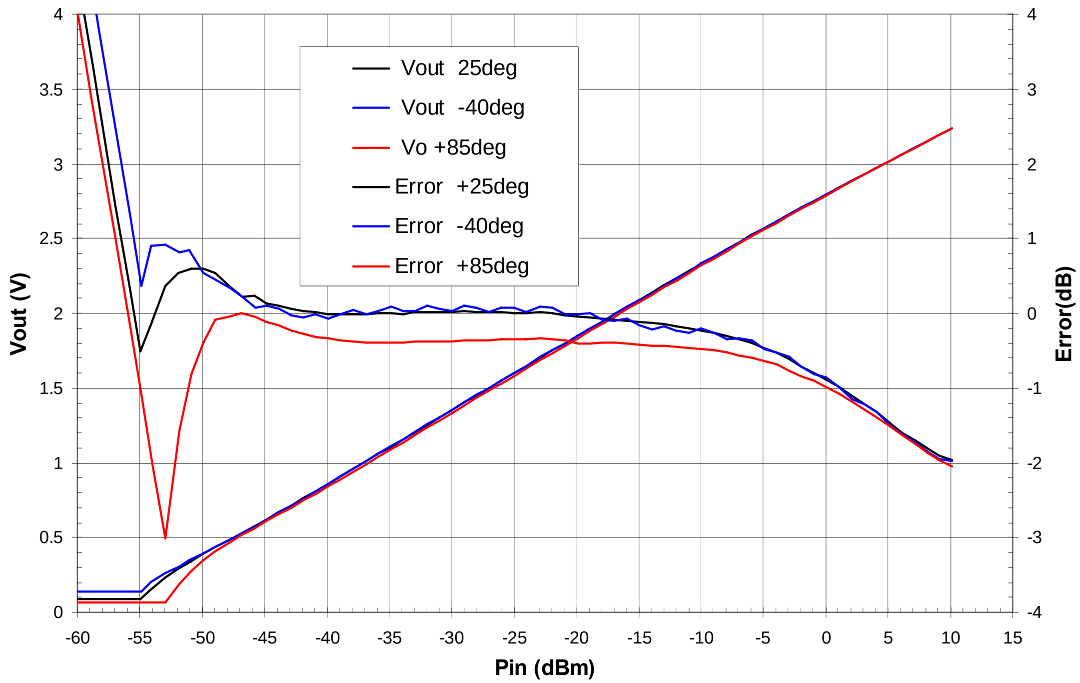
KEY SPECIFICATIONS

- Dynamic Range: >60dB
- Temperature Stability: +/-0.5dB
- Frequency Range: LF to 2.7GHz
- Package: 5x5mm 32 Lead LFCSP

FEATURES

- Dual channel and Difference Output Ports
- Integrated accurately scaled Temperature Sensor
- Linear-in-dB output

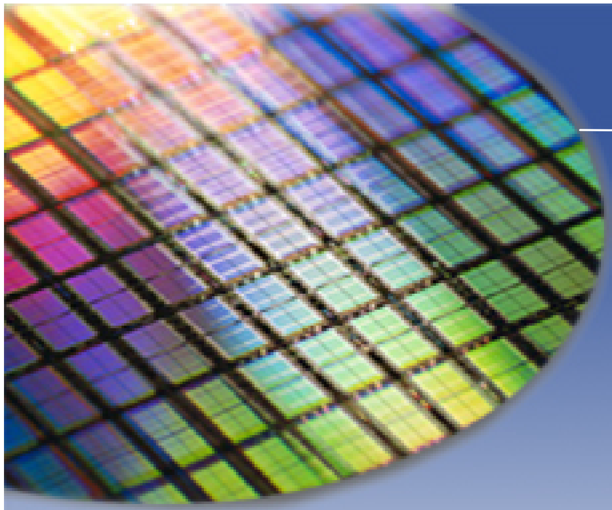
AD8364 RMS-DC Accuracy @ 2140 MHz -40 degC to +85 degC



TruPwr™ RMS Detectors

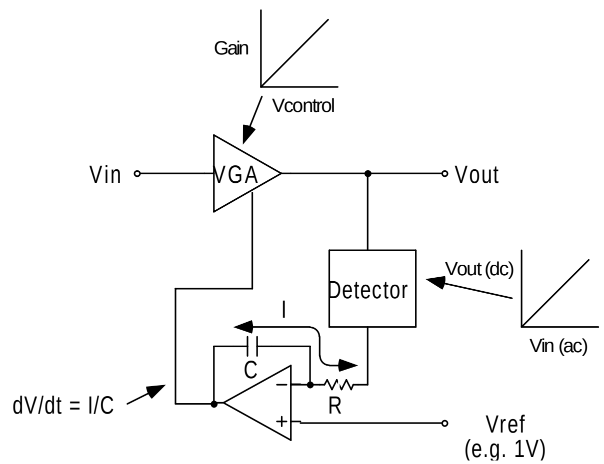
Modulation Independent RF Measurements

Part#	*RF Freq (MHz)*	*Dynamic Range (dB)*	*Temp Stability (dB)*	Voltage Supply (V)	Supply Current (mA)	Package
AD8361	*2500*	*30*	*±0.25*	**2.7 to 5.5**	**1.1**	**6-Lead SOT-23 8-Lead uSOIC**
ADL5501	*4000*	*30*	*±0.25*	**2.7 to 5.5**	**1**	**6-Lead SC-70**
AD8362	*2700*	*60*	*±1*	**4.5 to 5.5**	**20**	**16-Lead SOP**
AD8364 (Dual Channel)	*2700*	*60*	*±0.5*	**4.5 to 5.5**	**72**	**32-Lead LFCSP**



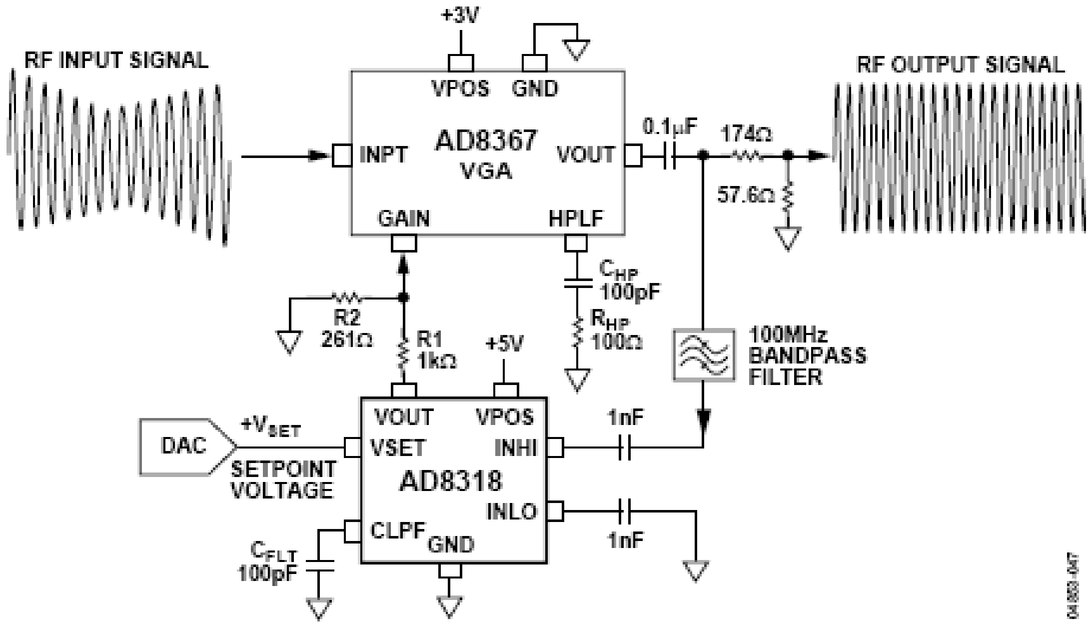
Controlling AGC Loops with RF Detectors

A Typical AGC Loop



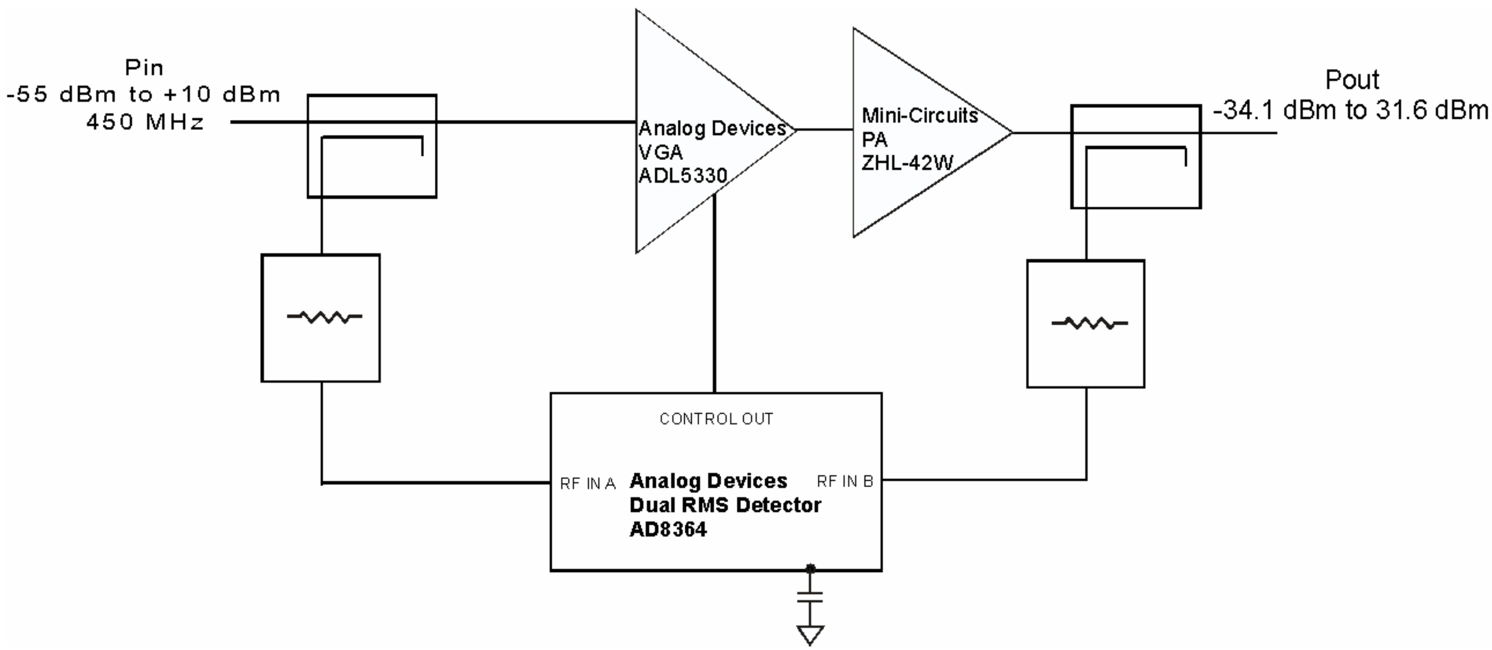
- **Detector measures output power from a variable gain amplifier or power amplifier**
- **Measured result is compared to a setpoint value**
- **Error amplifier/Integrator adjusts gain so that output power corresponds to setpoint**
- **Integrator capacitor/resistor set response time of loop**
- **Many of ADI's detectors have an integrated "Controller Mode"**

A Practical AGC Loop using a Log Amp



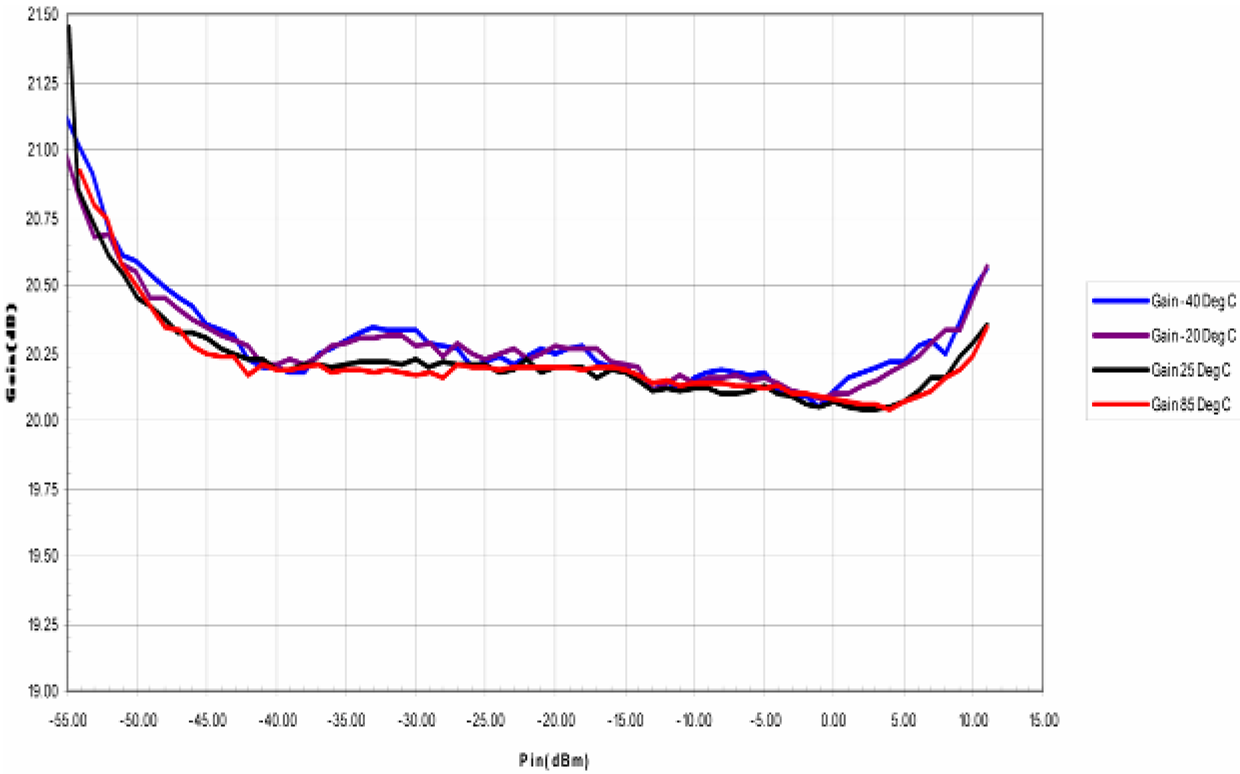
- Setpoint is applied to Detector VSET input
- Vout varies up or down to balance loop
- Use to set output to a fixed value (fixed VSET, variable input power) or to vary output power (variable VSET, fixed or variable input power)
- Set response time of loop by varying Cflt

Controlling Gain with a Dual RMS Detector



- **Dual RMS Detector can also operate in Controller Mode**
- **Detector measures and controls VGA in an analog loop**
- **Detector tries to balance input power at its two RF inputs**
- **Gain setpoint is controlled by difference in external attenuators**

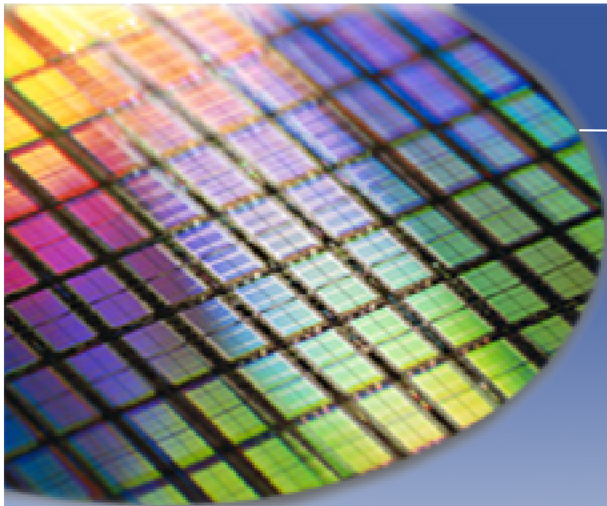
Gain vs. Input Power for Analog Gain Control Loop



- Gain varies by only +/-0.25 over a 60 dB input range
- Excellent stability over temperature

RF Detectors for Analog AGC Loops

Part No.	*RF Freq (MHz)*	*Dynamic Range (dB)*	Setpoint Voltage Range (V)	Comments
AD8311	*100 to 2500*	*50*	0.4 to 1.4	Wafer-Level CSP Package
AD8315	*100 to 2500*	*50*	0.4 to 1.4	
AD8316	*100 to 2500*	*50*	0.4 to 1.4	
AD8318	*1 to 8000*	*60*	0.5 to 2	Fast Responding
AD8317	*1 to 10000*	*50*	0.3 to 1.6	Fast Responding
AD8319	*1 to 10000*	*40*	0.3 to 1.5	Fast Responding
AD8362	*Low Freq to 2700 MHz*	*60*	0.4 to 3.5	RMS Responding
AD8364	*Low Freq to 2700 MHz*	*60*	0.25 to 3.5	Dual RMS Responding

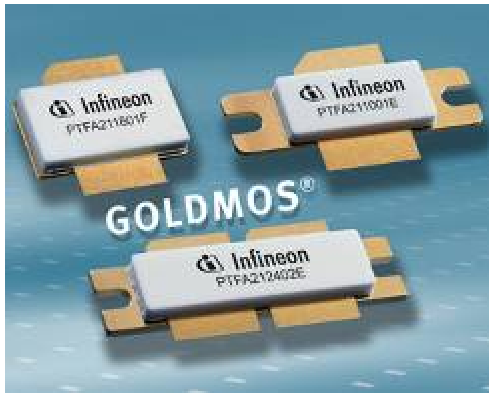


ADI 2006 RF Seminar

RF Components in High Power Amplifiers

ANALOG DEVICES

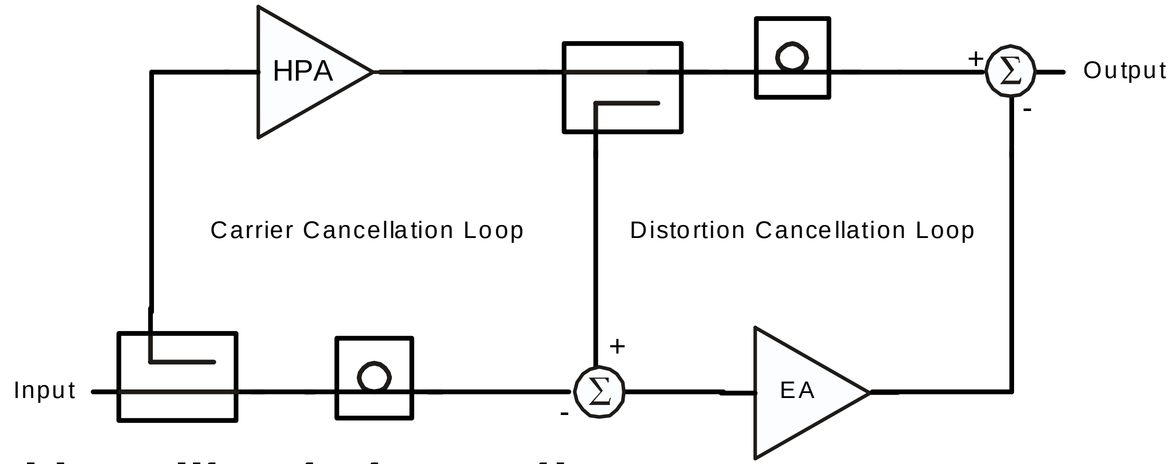
High Power Amplifiers



- Transmitter is usually segmented into a Radio and a Power Amplifier
- In order to operate as close as possible to the amplifier's compression point (higher efficiency), many HPAs incorporate circuitry which reduces distortion (Linearization)
- Popular Linearization techniques are Feed Forward, Feedback, Digital Pre Distortion and Analog Pre-Distortion

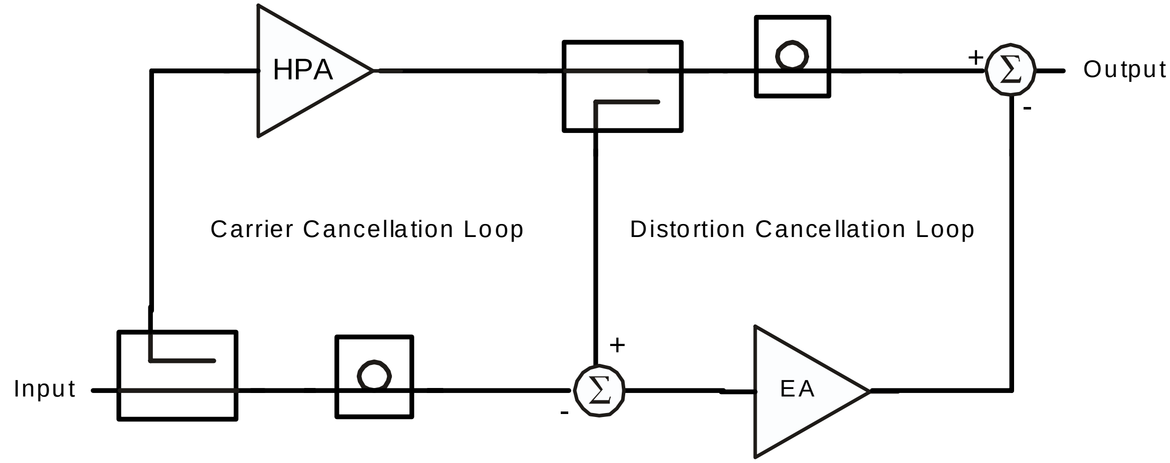
ANALOG DEVICES

A Simplified FFLA System – Carrier Cancellation



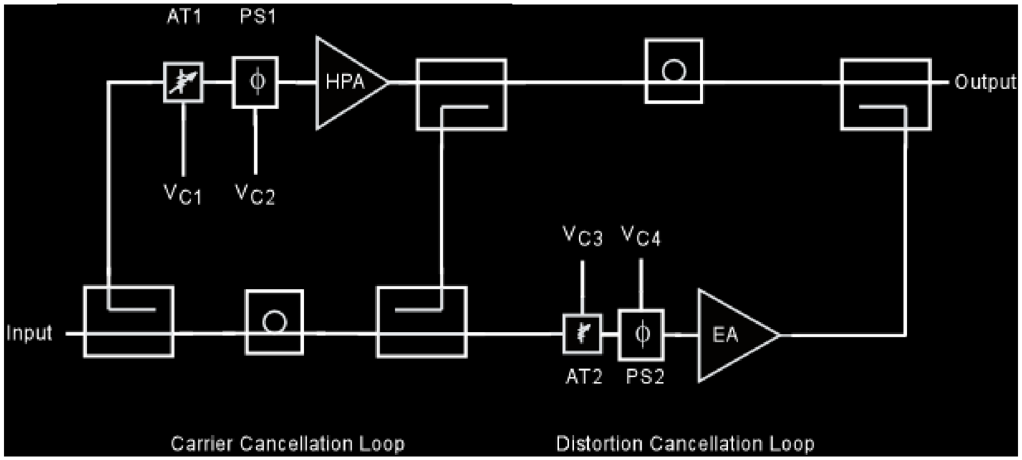
- Input signal is split onto two paths
- One path goes to input of High Power Amplifier (HPA)
- Output of amplifier comprised of amplified input signal and distortion generated within the HPA
- Distorted output signal fo the HPA is sampled and conveyed to one input of a differencing node
- Other input of the differencing node is the undistorted input signal, delayed by an interval equal to the delay of the HPA/sampled output path
- Output of the differencing node is distortion signal only

A Simplified FFLA System – Distortion Cancellation



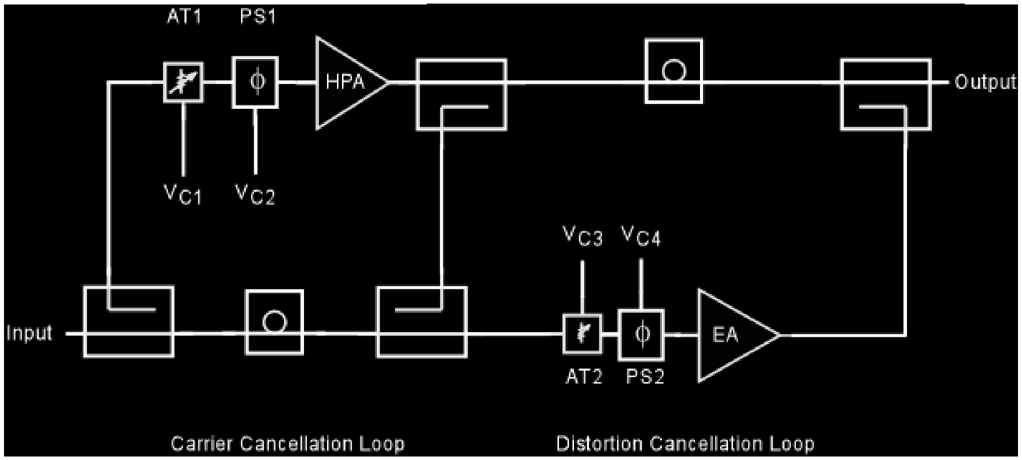
- Distortion signal is amplified by a very linear error amplifier (EA)
- Output of EA is applied to one input of another differencing node
- Other input to differencing node is the distorted output of the HPA, delayed by an interval equal to the carrier cancellation sampling path and the EA path
- Distortion present in the output of the HPA is cancelled in this differencing node
- Ideal output of differencing node is amplified, undistorted carrier

A Practical FFLA with Adjustments – 1st Loop



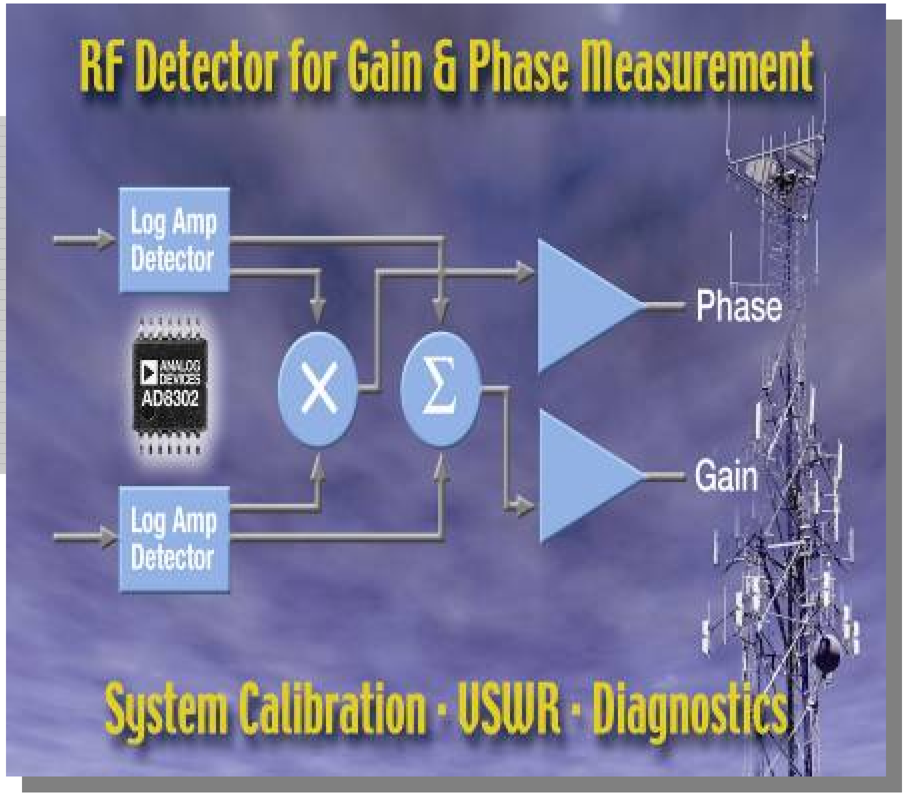
- **In the Carrier Cancellation Loop, a voltage variable attenuator (VVA) and a variable phase shifter (VPS) are put in cascade with the input to the HPA**
- **VVA and VPS are used to optimize carrier cancellation at the input to the EA**
- **Control voltages to VVA and VPS are often static voltages, set at the factory, but may be adaptively controlled[1]**

A Practical FFLA with Adjustments – 2nd Loop



- In the Distortion Cancellation Loop, a VVA and a VPS are put in cascade with the input to the EA
- VVA and VPS are used to optimize distortion cancellation at the output of the FFLA system
- Control voltages to VVA and VPS are often static voltages, set at the factory, but may be adaptively controlled[1]

AD8302 – Gain / Phase Detector



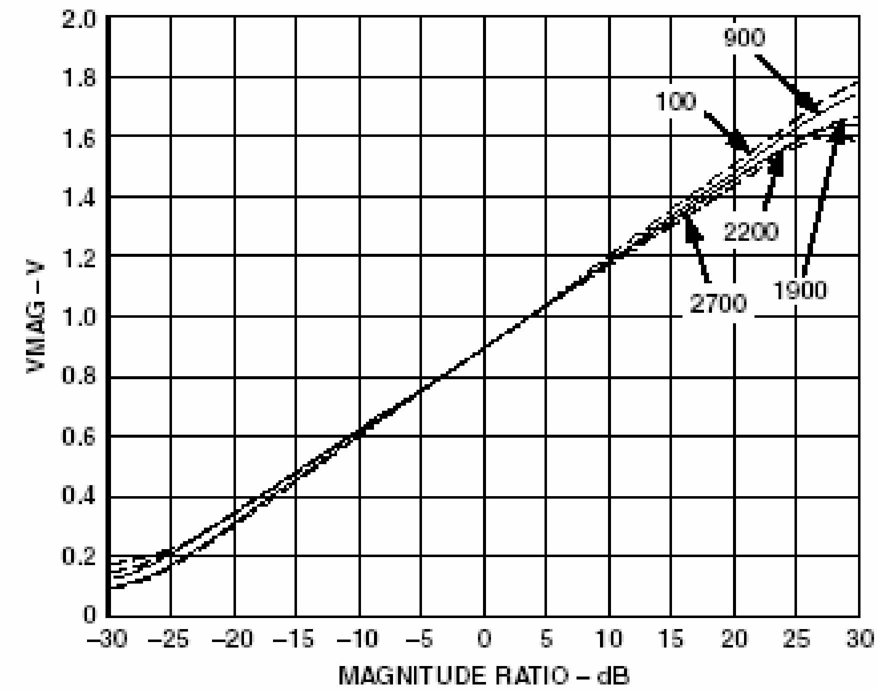
KEY SPECIFICATIONS

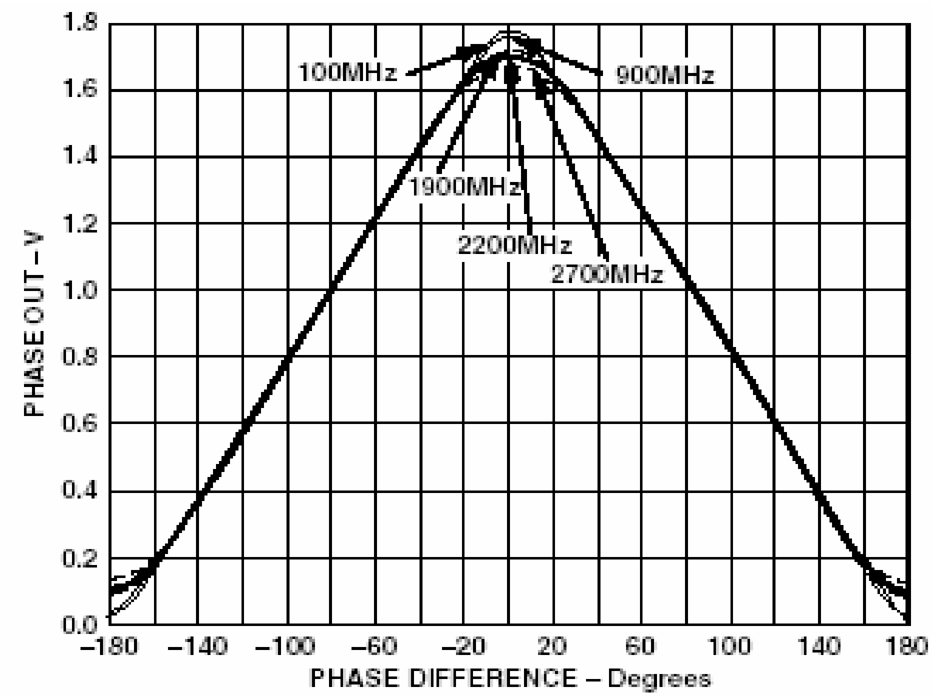
- Frequency Range: LF to 2.7 GHz
- Gain range: 60 dB, 30mV/dB, 0 to 1.8V
- Phase range: 180 deg, 10 mV/deg, 0 to 1.8V
- Package: 14-TSSOP

FEATURES

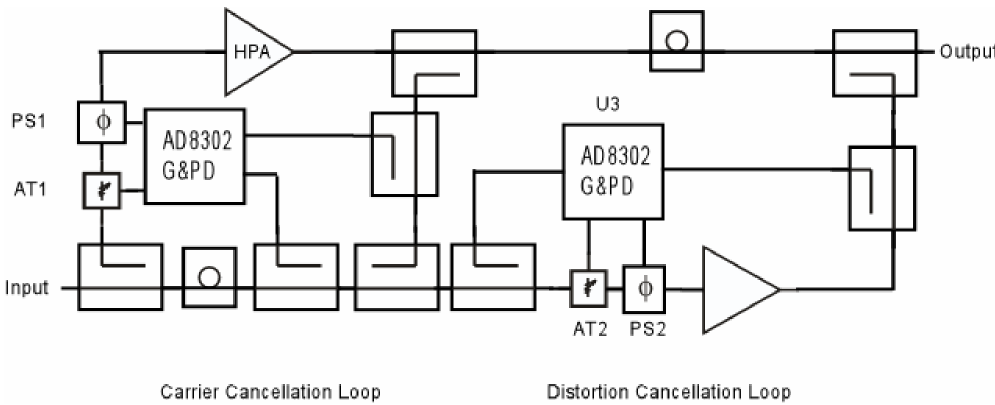
- Matched Log Amps for Temperature Stability
- Measurement and Control of Gain or VSWR

AD8302 – Gain/Phase Detector
Gain and Phase Transfer Functions





A Complete Feedforward Linearized Amplifier

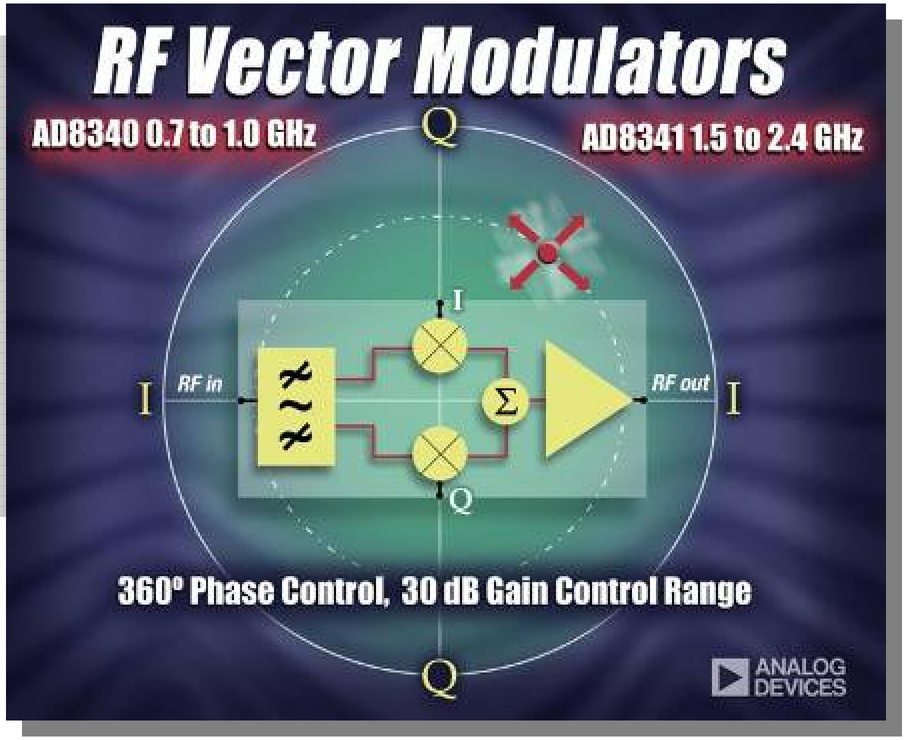


- **AD8302 GPD can be used to control both loops of the FFLA**
- **AD8302 used to control VVA and VPS in Carrier Cancellation loop to control cancellation of carrier at the input to the EA**
- **AD8302 used to control VVA and VPS in Distortion Cancellation loop to control cancellation of intermodulation sidebands at FFLA Output**

AD8340 and AD8341 Vector Modulator

KEY SPECIFICATIONS

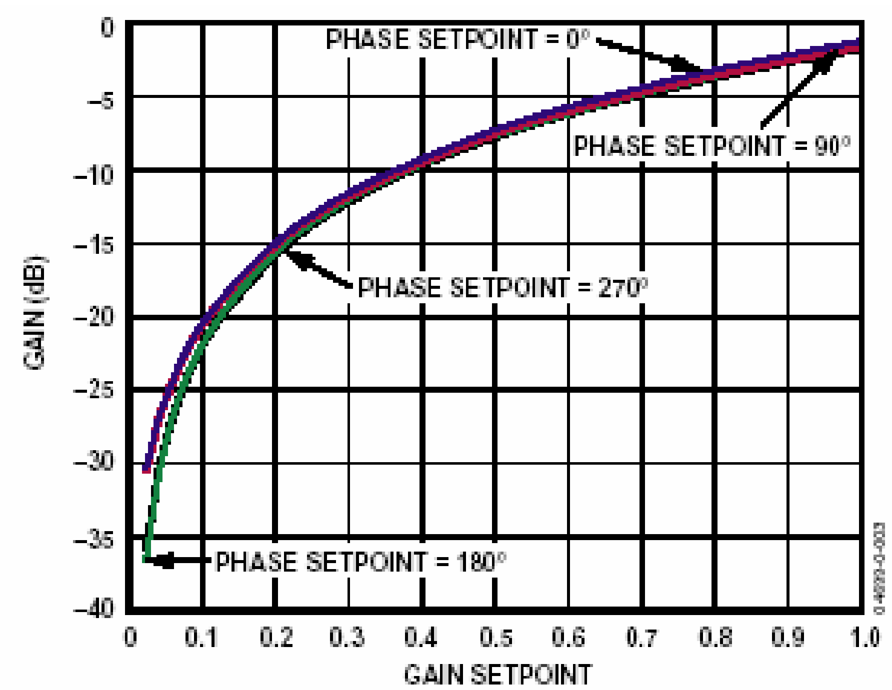
- RF Bandwidth 0.7 – 1.0GHz / 1.5 – 2.4 GHz
- Gain control range: -32dB to -2dB
- Phase control range: continuous 360°
- Output IP3: 24dBm / 22dBm (max gain)
- Output Noise: -149 dBm/-151Hz
- Package 4x4mm 24-LFCSP

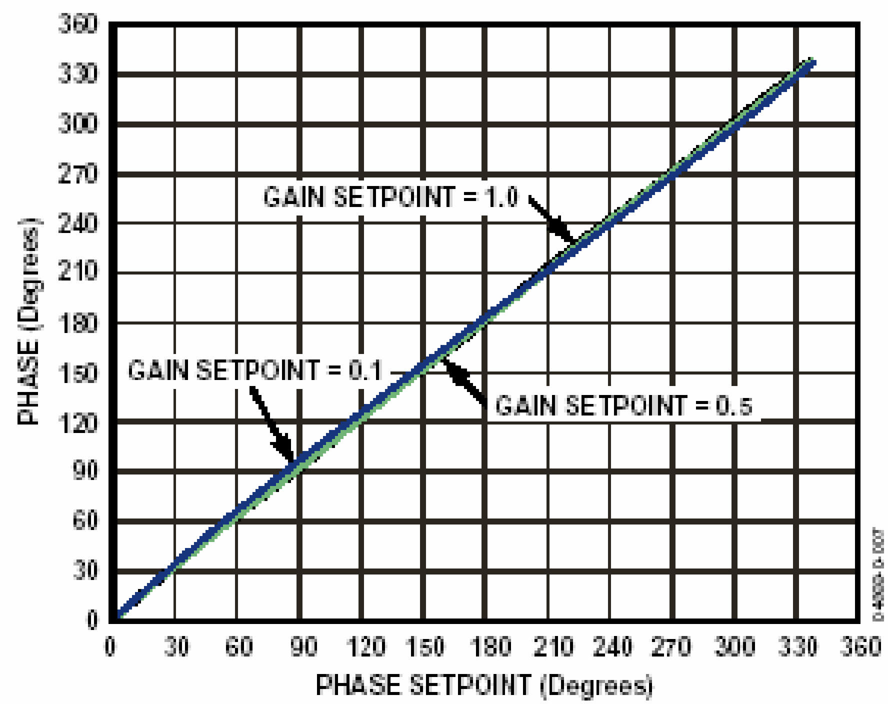


FEATURES

- Amplitude and Phase Modulator inputs
- Modulation by Cartesian I and Q
- Output power disable function: 40dB, 10ns

AD8340 Vector Modulator – Gain and Phase Control





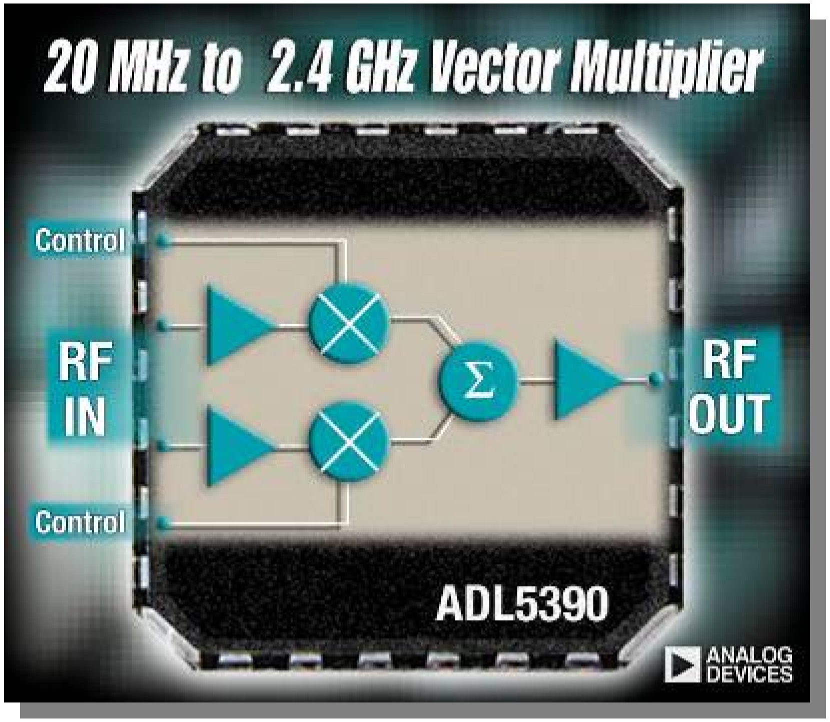
880 MHz

- ❑30 dB Gain Control Range
- ❑360 degree Phase Control Range

ADL5390 RF / IF Vector Multiplier

KEY SPECIFICATIONS

- Bandwidth 20MHz to 2.4GHz
- Continuous Amplitude Control +5 to –30dB
- Wide band 230MHz Cartesian Interface
- OIP3 +25dBm
- Output P1dB +13dBm
- Output Noise Floor –150dBm/Hz
- Package 4x4mm LFCSP



FEATURES

- Output Switch Disable 40dB, 10ns

Components for PA Feedforward Linearization

Vector Modulators

Part No.	RF Freq (MHz)	IQ Bandwidth (MHz)	Noise Floor (dBm/Hz)	P1dB (dBm)	Power Supply (mA)	Package
AD8340	700 to 1000	230	-149	11	130	24-lead CSP
AD8341	1500 to 2400	230	-151	8.5	130	24-lead CSP
ADL5390	20 to 2400	230	-150	+13	130	24-Lead LFCSP

Gain/Phase Detector

Part No.	RF Freq (MHz)	Dynamic Range (dB)	Accuracy (dB)	Response Time (ns)	Package Type	Comments
AD8302	>0 to 2700	60	±0.2	60	14-lead TSSOP	Dual channel gain and phase detector

ANALOG DEVICES